

Title	Page
Cover Sheet	1
Block Diagram	2
CPU-CLK/Control/MISC/PEG ,CPU-DMI	3,4
CPU-Memory 0/1/2/3	5,6
CPU-Power,CPU-GND/RSVD	7,8
DDR III DIMM 1 / 2,DDR III DIMM 3 / 4	9,10
PBG-PCI /E/DMI /USB/CLK	11
PBG-SATA/HOST/FAN/GPIO/CCMOS	12
PBG-SMB/LPC/AUDIO/RTC	13
PBG-POWER,GND/NVRAM	14
PBG-STRAP PIN	15
SATA PORTS,FAN CONTROL	16
PCIE Slot X16 /X16 /X1 /X1	17,18
SIO-F71889AD/KB	19
USB CONNECTOR X2	20,21
UPD720200F1 USB3.0 X2	22,23
USB3.0 CONNECTOR & POWER X2	24
USB FULL CHARGER	25
CLK GEN 932SQ420D ,BUFFER 9FG1216	26
Audio ALC892 , LAN RTL8111E	27,28
ATX/Front Panle,ACPI Controller UPI	29,30
VRD12-uP1618 - 6+2 Phase	31
VRD12-uP6234 - 1 Phase SA(Dr.MOS)	32
VRD12-uP6275 - 4 Phase to 8Phase	33
VRD12-uP1618 Dr.MOS - 8Phase	34
PCH Power - uP1504 - 1 Phase	35
VTT Power - uP1504 - 1 Phase	36
DDR Power - uP1504 - 1 Phase X2	37,38
OC SWITCH & W604GPIO CTL	39

Title	Page
PHASE DROPPING / LED	40
EMI Solution For power	41
XDP / Manual Parts	42
GPIO SETTING/PCI ROUTING	43
SIO GPIO SETTING	44
POWER MAP	45
POWER SEQUENCE	46
HISTORY	47

# MS-7738

## M-ATX

Ver: 1.0

### CPU:

INTEL - Sandy Bridge-E LGA2011

### System Chipset:

INTEL - Patsburg PCH

### OnBoard Chipset:

Clock Gen:932SQ420D + 9FG1216

LAN:RTL 8111E 10/100/1000 NIC X 1

USB3.0: UPD720200F1

Flash ROM: 64 MB SPI (PCH)

SIO:FIN71889AD(LAA)

### Expansion Slots:

PCI Express (X16) Slot \* 2

PCI Express (X1) Slot \* 2

### Main Memory:

DDRIII (1066/1333MHz) \* 4

### PWM:

CPU:uP1618 (8-Dr.MOS)

CPU\_SA:uP1618 (1-Dr.MOS)

CPU\_VTT:UP1504 (4-package)

VCC\_DDR:UP1504 (4-package)

PCH:uP1504 (4-package)

### Other:

SATA3.0 x2+SATA2.0 x4 (PCH)

USB2.0 \*10 (Rear\*6 Front\*4)

USB3.0 \*4 (Rear\*2 Front\*2)

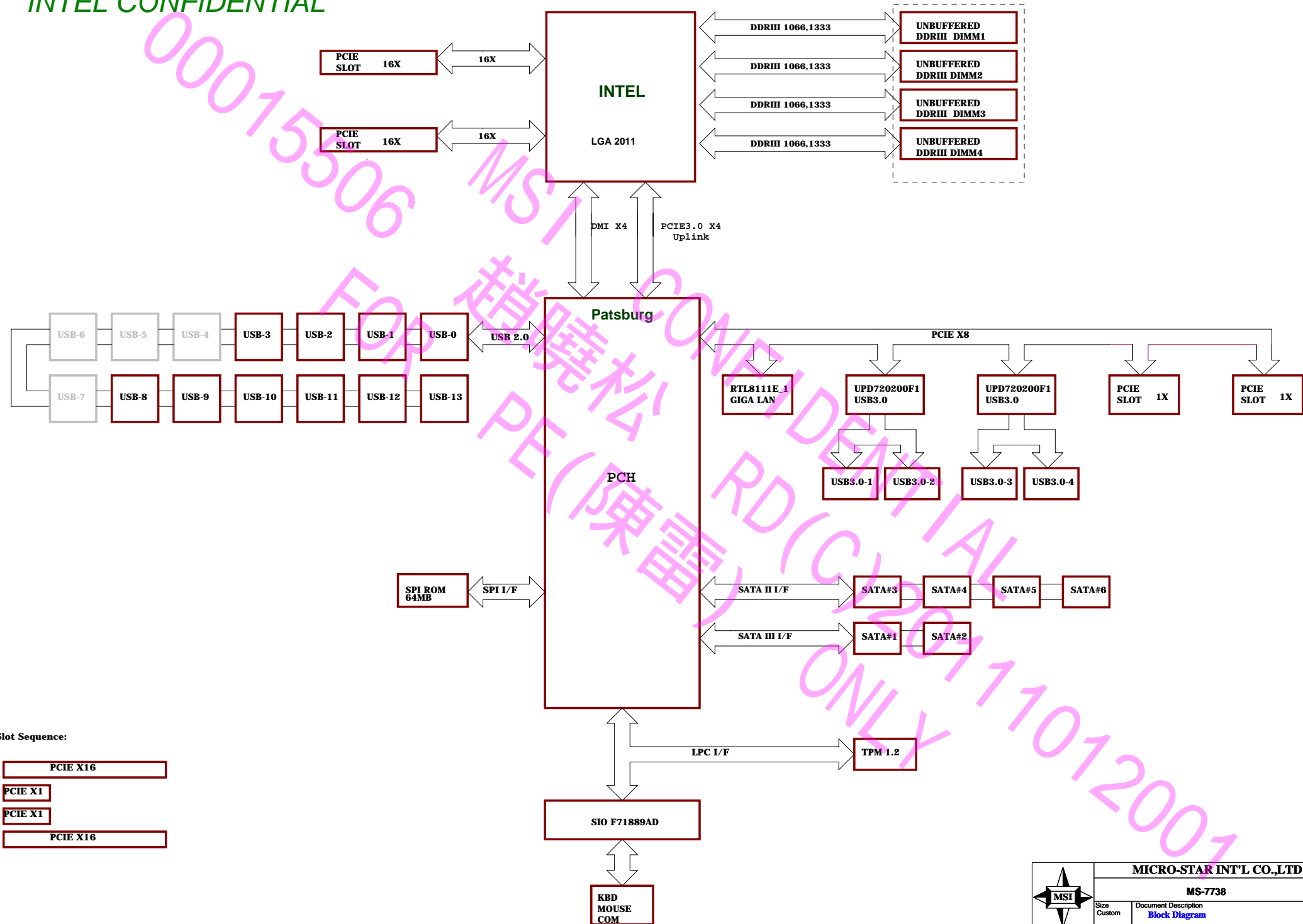
COM Header \*1

### ACPI:

UPI



MICRO-STAR INT'L CO.,LTD			
MS-7738			
Size Custom	Document Description Cover Sheet		Rev 10
Date: Thursday, September 08, 2011	Sheet	1	of 47

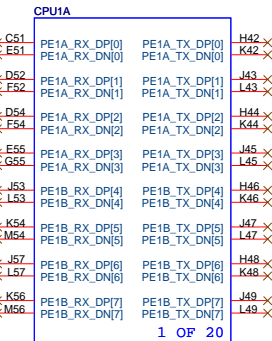


MICRO-STAR INT'L CO.,LTD

MS-7738

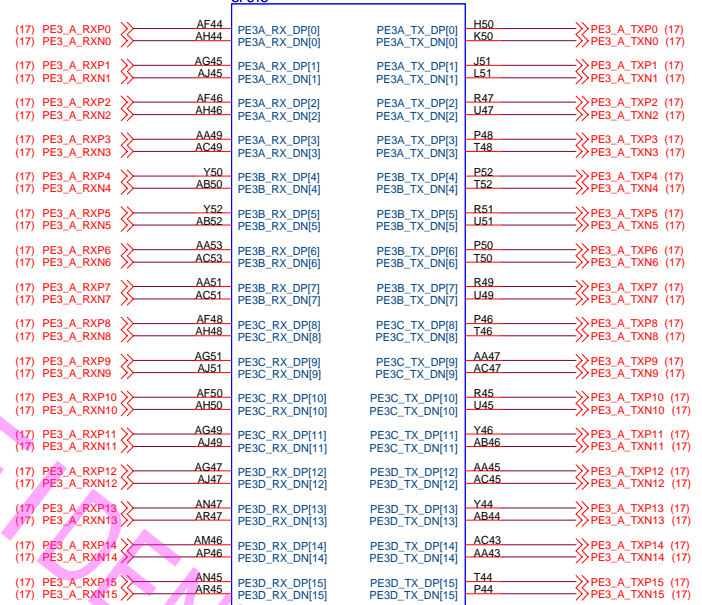
Size Custom	Document Description Block Diagram	Rev 10
Date: Monday, September 26, 2011	Sheet 2 of 47	



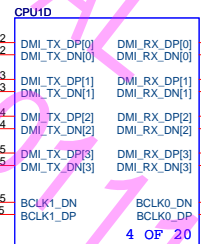


LGA2011

PE1A : X4 UPLINK  
PE1B : X4 SLOT



LGA2011



LGA2011



MICRO-STAR INT'L CO.,LTD

MS-7738

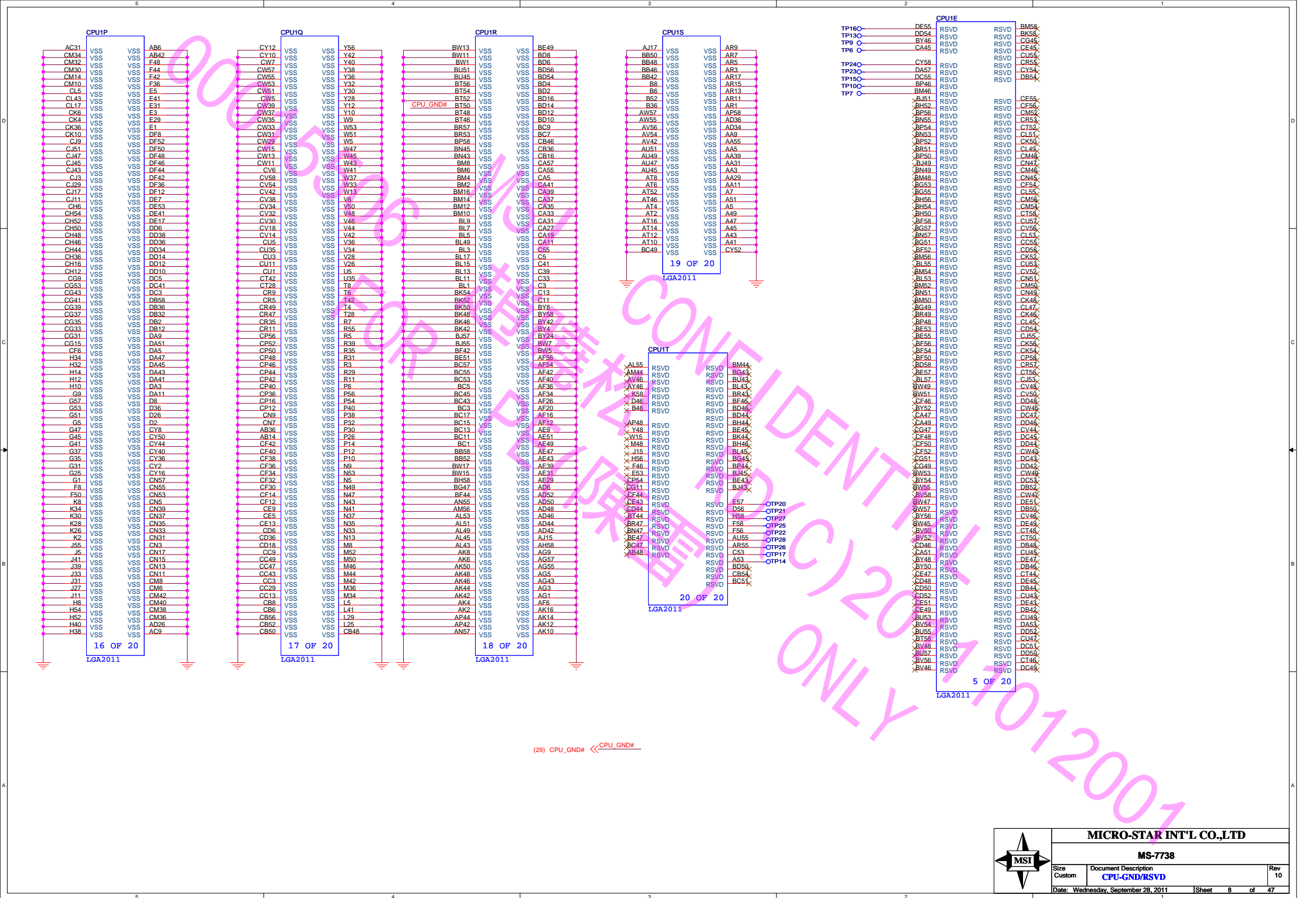
Size	Document Description	Rev
Custom	CPU-PEG/DMI	10
Date:	Wednesday, September 28, 2011	Sheet 4 of 47







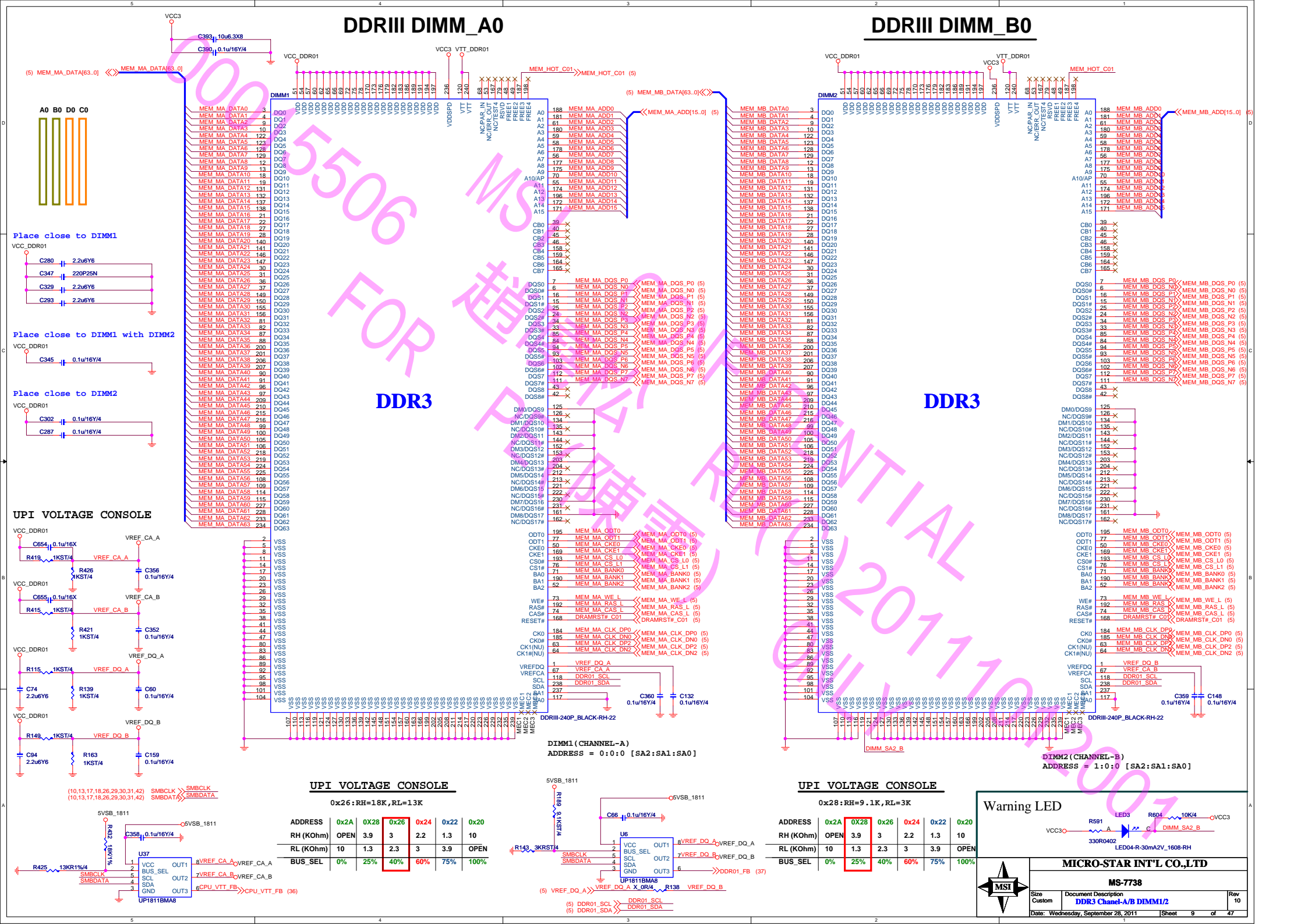






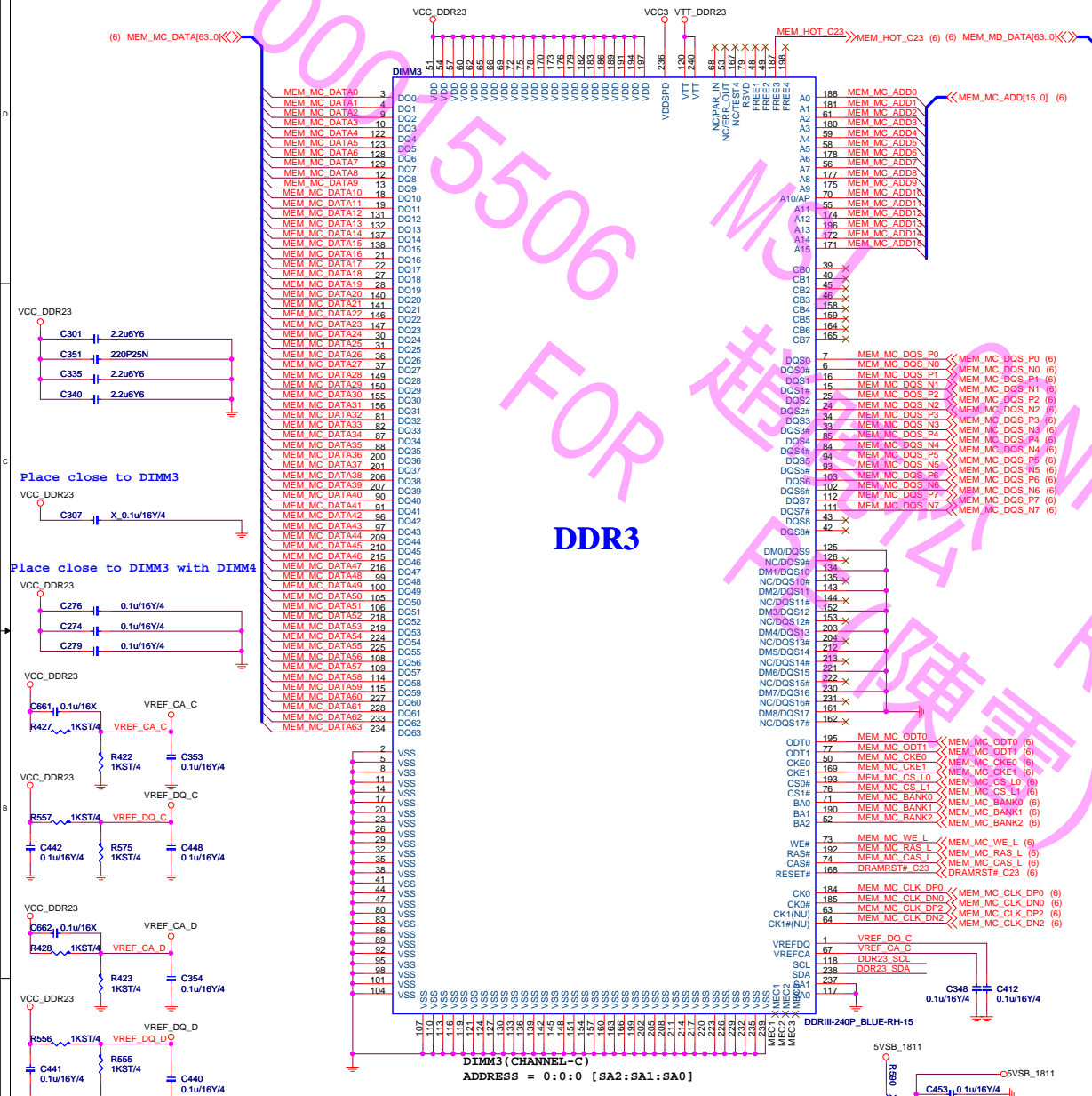
# DDR3 DIMM\_A0

# DDR3 DIMM\_B0



# DDR3 DIMM\_C0

# DDR3 DIMM\_D0



DDR3

DDR3

## UPI VOLTAGE CONSOLE

0x20:RH=10K

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (Kohm)	OPEN	3.9	3	2.2	1.3	10
RL (Kohm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

(6) VREF\_DQ\_C >> VREF\_DQ\_C X 0R/4 R564 VREF\_DQ\_D

(6) DDR23\_SCL >> DDR23\_SCL  
(6) DDR23\_SDA >> DDR23\_SDA

## UPI VOLTAGE CONSOLE

0x2A:RL=10K

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (Kohm)	OPEN	3.9	3	2.2	1.3	10
RL (Kohm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

## Warning LED

VCC3 >> LED1 >> VCC3  
330R/402



MICRO-STAR INT'L CO.,LTD

MS-7738

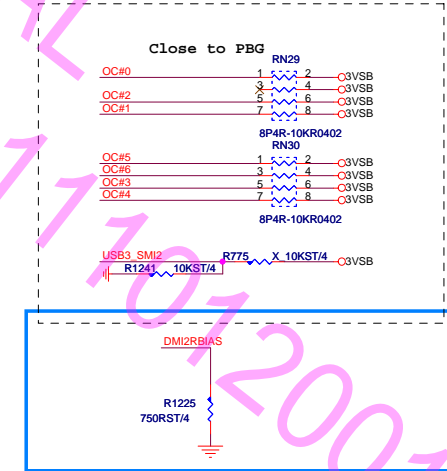
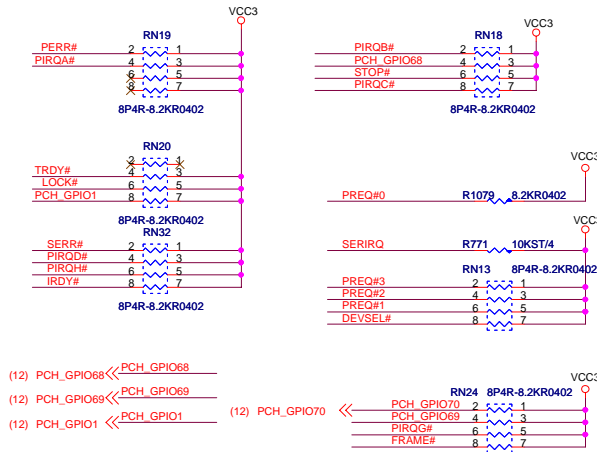
Size Custom Document Description

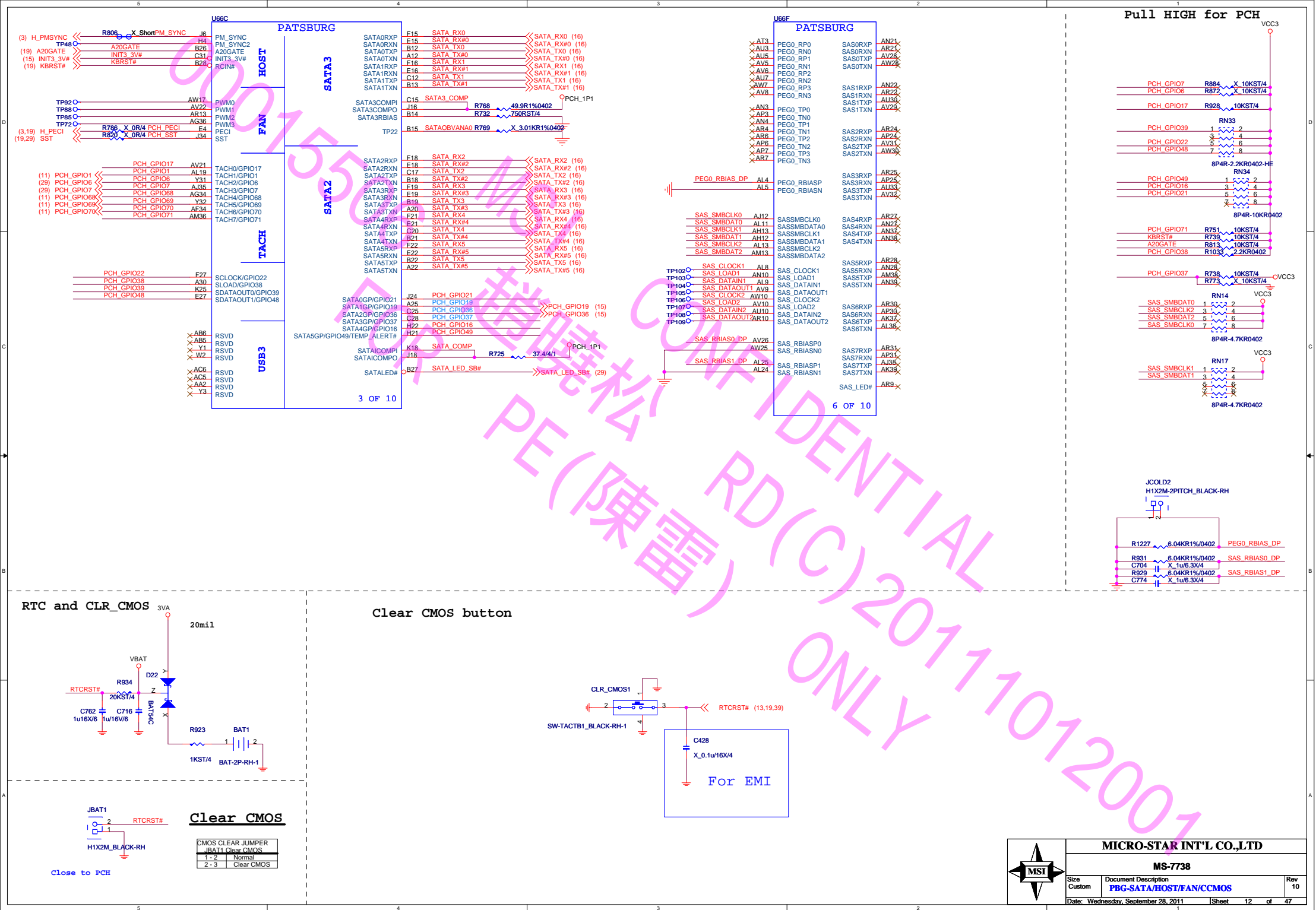
DDR3 Chan-C/D DIMM3/4

Date: Wednesday, September 28, 2011

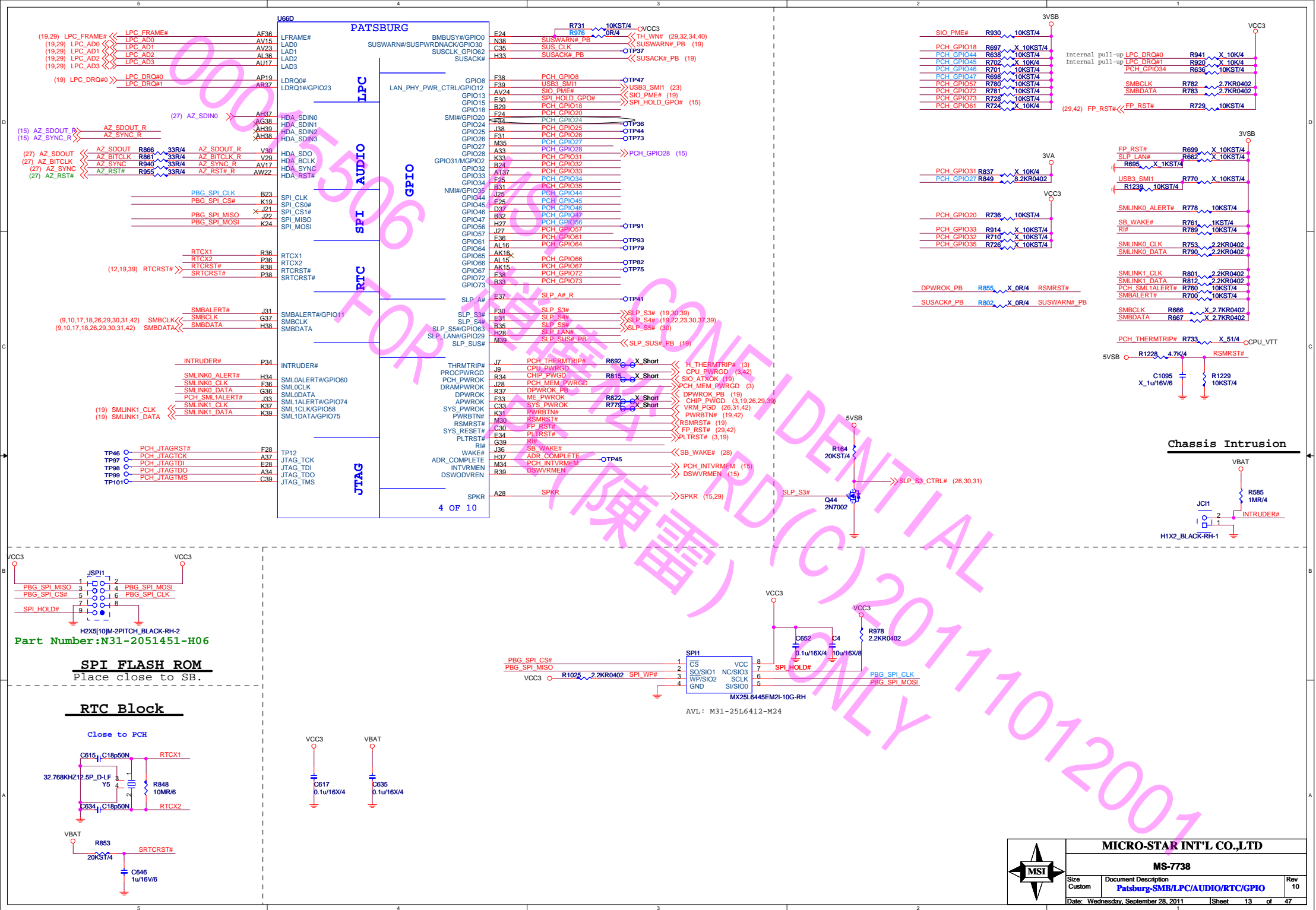
Sheet 10 of 47

# PCI PULL-UP / DOWN RESISTORS

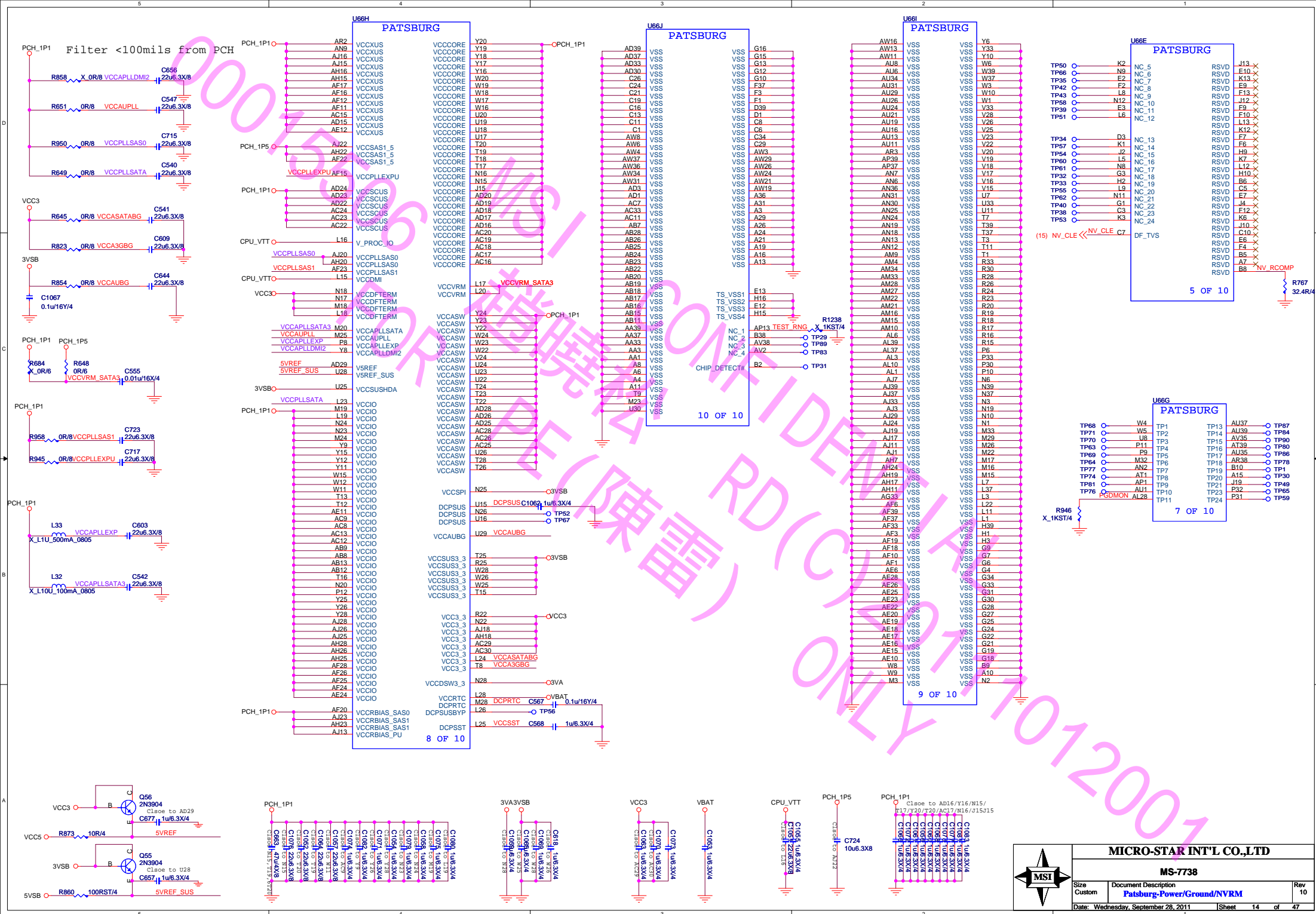






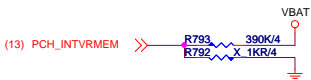
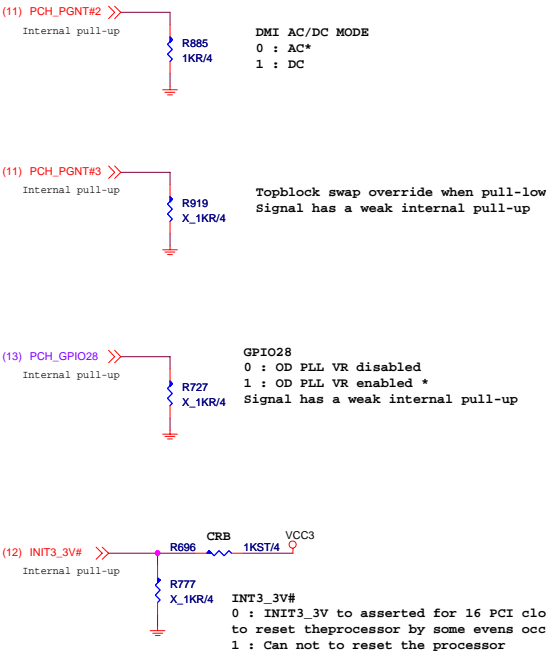
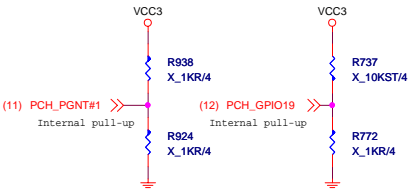






PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

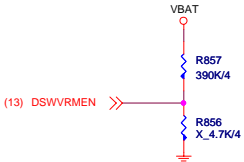


INTVRMEN

0 : DISABLE INTERNAL VRM

1 : ENABLE INTERNAL VRM \*

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

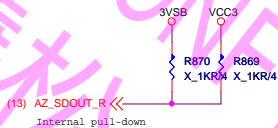


DSWVRMEN

0 : Disable Internal Deep Sleep 1.05 V regulators.

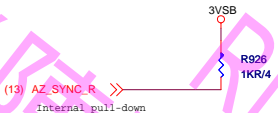
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must be connected even when not supporting DSW.



HDA\_SDO

Disable ME in Manufacturing Mode when pull LOW ????



HDA\_SYNC

OD PLL VR SUPPLY SEL

0 : 1.8V SUPPLY

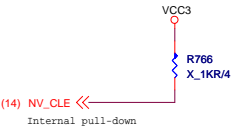
1 : 1.5V SUPPLY \*



GPIO15

0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY \*

1 : TLS CIPHER SUITE WITH CONFIDENTIALITY

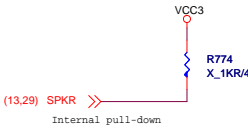


DMI/FDI TERMINATION VOLTAGE

DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH

DC COUPLED: TX/RX TO VSS IF SAMPLED LOW \*\*

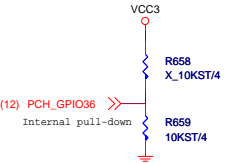
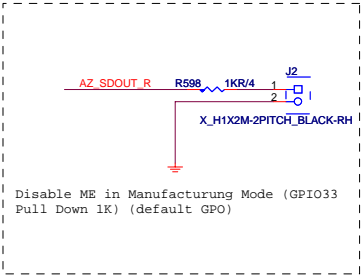
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



SPKR

0 : EN TCO REBOOT \*

1 : DIS TCO REBOOT



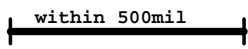
MICRO-STAR INT'L CO.,LTD

MS-7738

Size	Document Description	Rev
Custom	Patsburg -Strap	10
Date:	Wednesday, September 28, 2011	Sheet 15 of 47







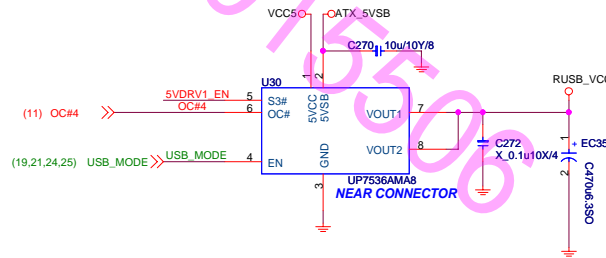
<b>MICRO-STAR INT'L CO.,LTD</b>			
<b>MS-7738</b>			
Size Custom	Document Description <b>PCI-E X16 Slot &amp; X4</b>		Rev 10
Date: Wednesday, September 28, 2011		Sheet 18 of 47	



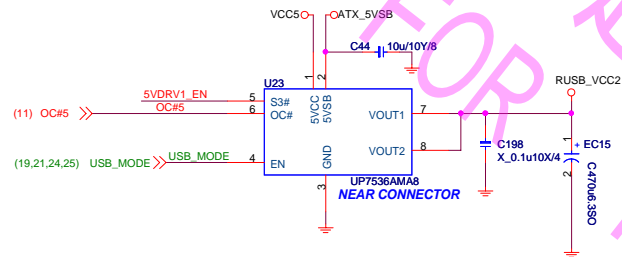


# Rear USB Connector

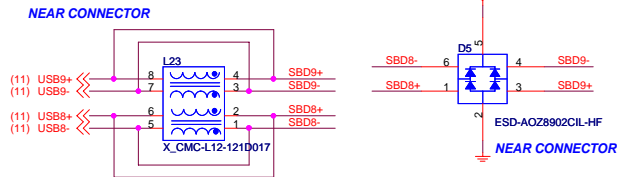
## USB POWER FOR PORT 8,9



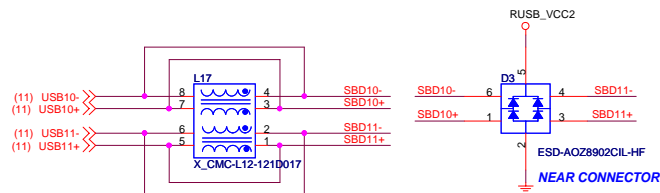
## USB POWER FOR PORT 10,11



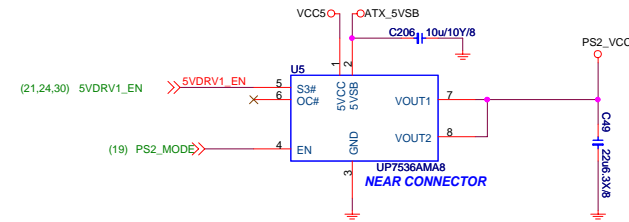
## REAR USB PORT 8,9 (With LAN)



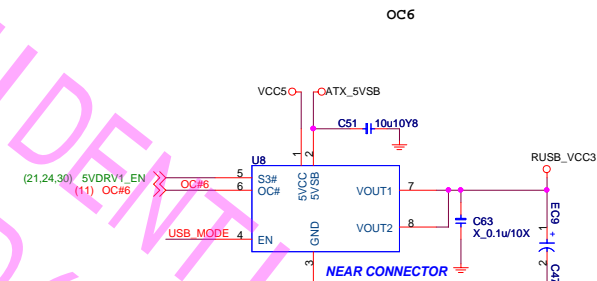
## REAR USB PORT 10,11



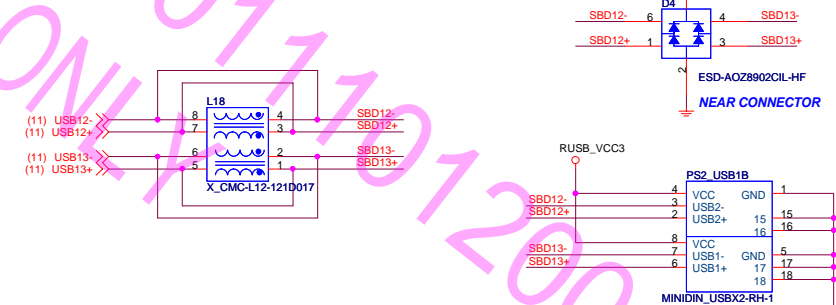
## PS2 POWER



## USB POWER FOR PORT 12,13



## REAR USB PORT 12,13 (WITH PS2)

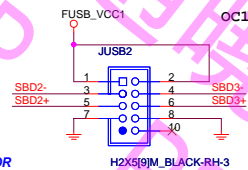
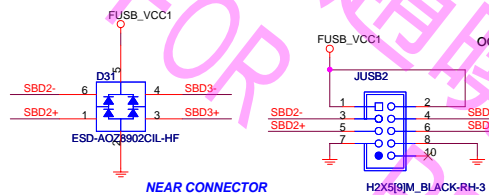
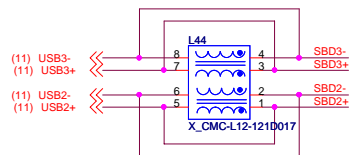


MICRO-STAR INT'L CO.,LTD

MS-7738

Size	Document Description	Rev
Custom	USB Connectors - 2	10
Date: Wednesday, September 28, 2011	Sheet 20 of 47	

### FRONT USB PORT 2,3

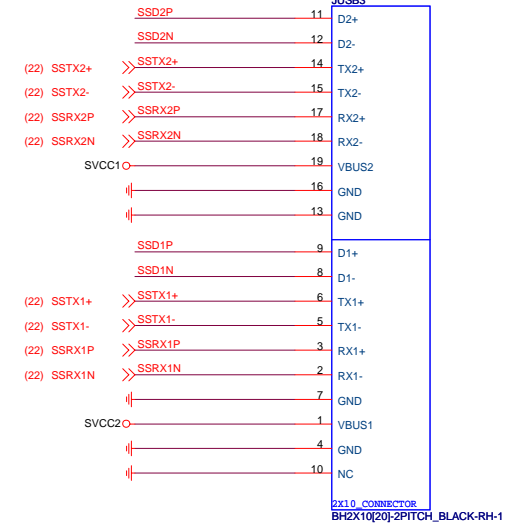
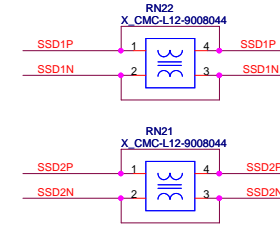
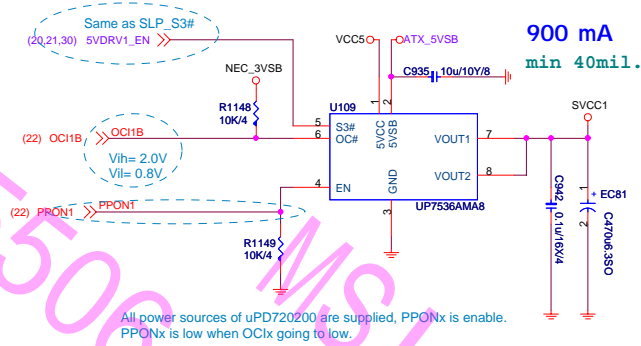




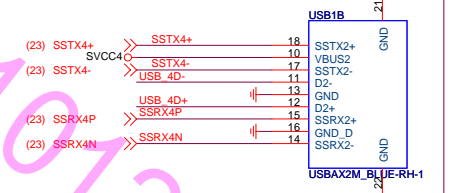
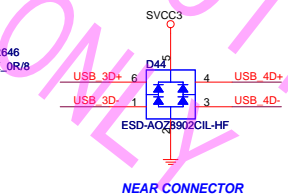
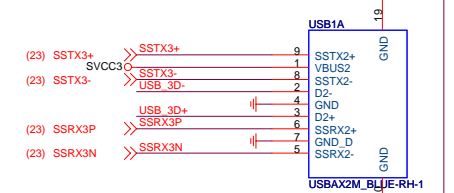
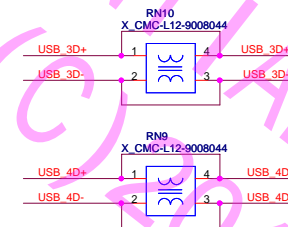
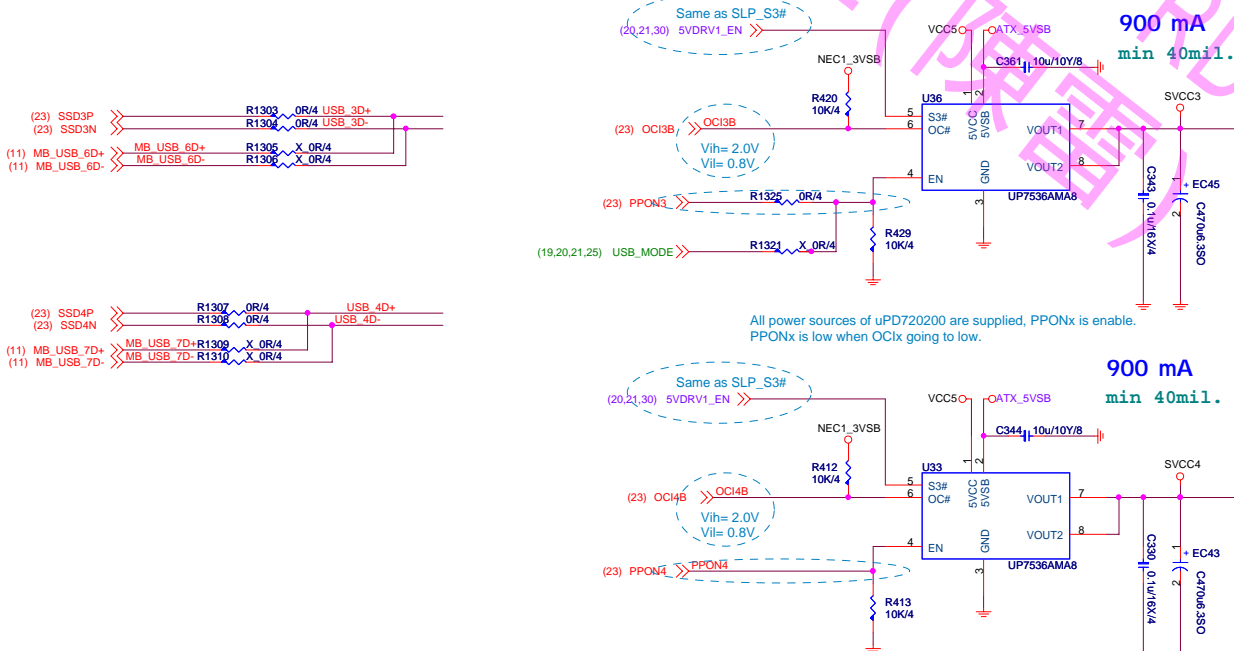




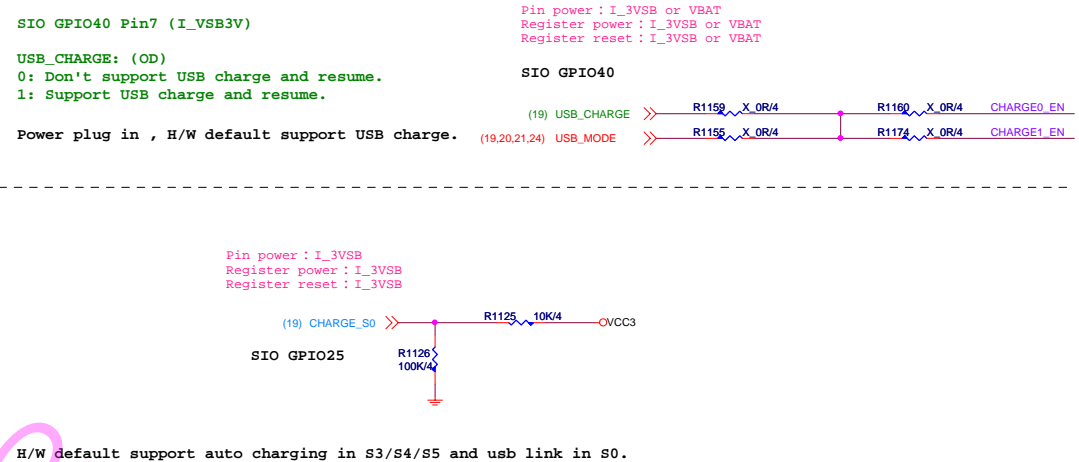
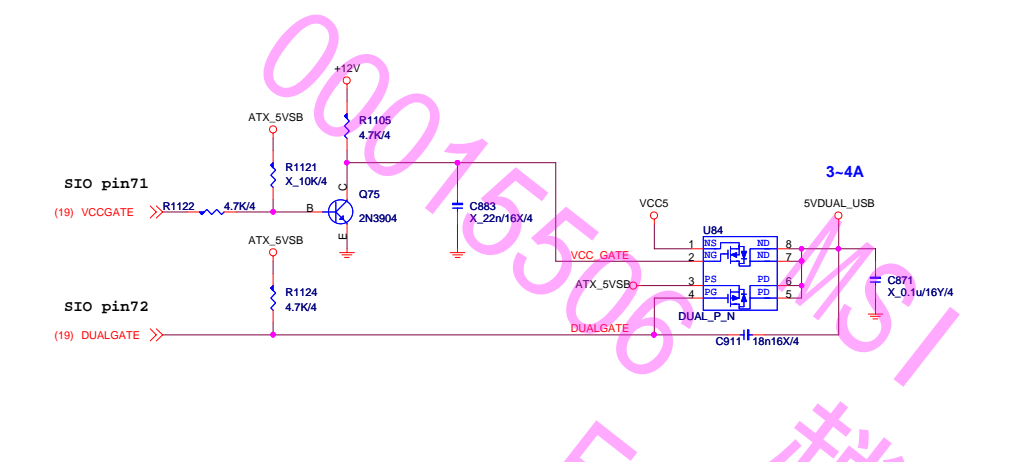
## FRONT USB PORT 4,5



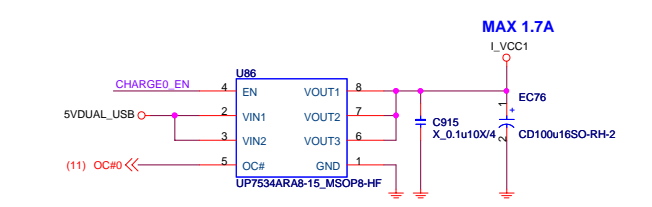
## REAR USB PORT 6,7



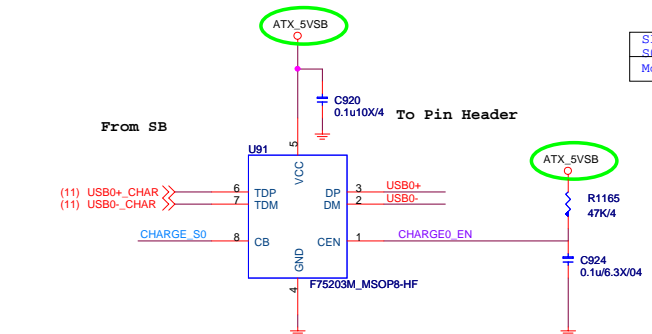
5VDUAL\_USB



USB POWER PORT 0 For USB Charging

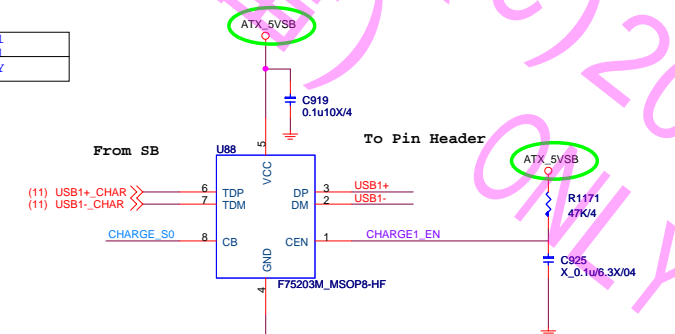
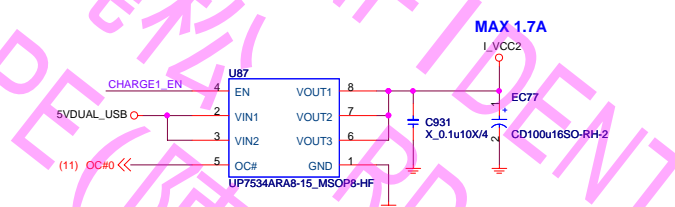


\*\* If your spec will not need bom option, please don't co-lay blue labels.

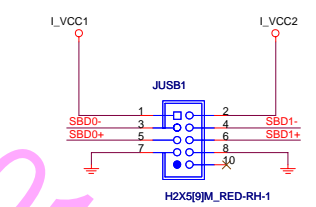
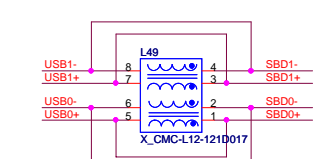


S1	0		0	1
S0	0		1	1
Mode	AUTO		A	Y

USB POWER PORT 1 For USB Charging



FRONT USB PORT 0,1



Please name the pin header JUSB1 and use SB USB0,1 link for charger port.

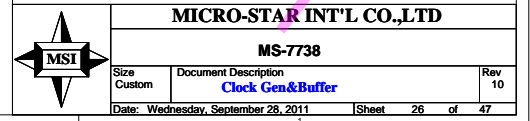
PI5USB14550 has internal EDS diode.

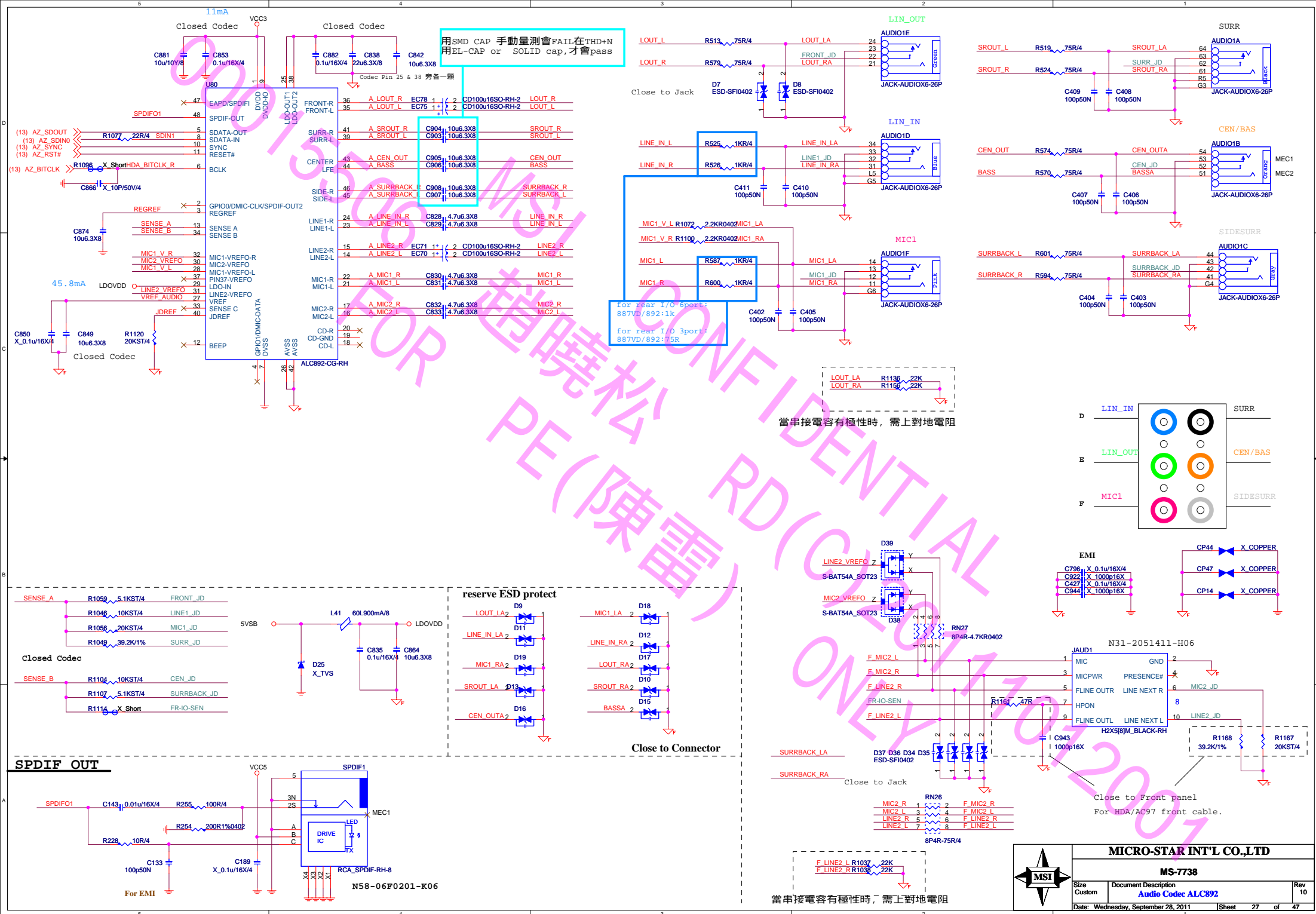
A type

2.70V< D+ <3.1 V ,

1.85V< D- < 2.1V.

For i-Pad / i-Phone 4G charges current up to 1.6A.









The schematic diagram illustrates the electrical connections for two modules, JFP2 and JFP1. JFP2 (H2X4[7]M\_BLACK-RH) features a speaker, buzzer, and three LEDs (SUS\_LED, PWR\_LED, EMI). JFP1 (H2X5[10]M\_BLACK-RH) includes a buzzer, three LEDs (SUS\_LED, PWR\_LED, IDE\_LED), and several pins (HDD+, IDE+, RESET+, PSIN#, NC). The diagram shows connections to various components like resistors, capacitors, and a buzzer. Key components include: JFP2 (H2X4[7]M\_BLACK-RH), JFP1 (H2X5[10]M\_BLACK-RH), D33 (1N4148S), RN23 (150R/8P4R), C947 (X 0.1u/16V/4), C946 (X 0.1u/16V/4), C937 (X 0.1u/16V/4), C941 (0.1u/10X/4), C938 (X 0.1u/16V/4), C939 (X 0.1u/16V/4), C940 (X 0.1u/16V/4), R1179 (X 0R/4), R1166 (33R/4), R1162 (330R/6), R1170 (10K/4), R1164 (4.7K/4), R1163 (100R/4), D32 (SATA LED), and D31 (SATA LED). The diagram also shows connections to various pins like SUS\_LED, PWR\_LED, EMI, HDD+, IDE+, RESET+, PSIN#, NC, and IDE\_LED. The diagram is labeled with (13,15) and (12) SATA\_LED\_SB# and (12) SATA\_LED\_SB#.

[illegible]

(19) TURBO\_MODE# <<< TURBO\_MODE#

3VSB

R334  
20K/4

JTURBO1

H2X214M BLACK-RH

Reserve pull high to 5VDIMM if PM don't want FLED light in deep mode.

[illegible]

Pin Name	Pin Number	Value	Component
VCCP	C385	22u6.3X/8	CPU_CORE
CPU_VTT	C391	22u6.3X/8	CPU_IO
CPU_SA	C386	22u6.3X/8	CPU_SA
VCCA_0	C509	22u6.3X/8	CPU_PLL
/CC_DDR01	C383	22u6.3X/8	DDR_A
/CC_DDR23	C378	22u6.3X/8	DDR_C/D
PCH_L1P1	C373	22u6.3X/8	PCH_L1P1V
PCH_L1P5	C445	22u6.3X/8	PCH_L1P5V

(3,13,19,26,39) CHIP\_PWDG>> G2

SKT\_D D1

(8) CPU\_GND>> G1

5VSB R1244 X 47K

Q84

D2 D1

S2 SKT\_D

X\_NN-2N7002D

The schematic shows the ATX\_V5VSB power supply regulation circuit. It includes two MOSFETs, Q4 (N-channel) and Q5 (P-channel), both from X\_2N7002. The gate of Q4 is driven by the TH\_CTRL signal through R1240 (47k). The source of Q4 is connected to ground through R1243 (47k). The drain of Q4 is connected to the ATX\_V5VSB input through R1271 (47k). The gate of Q5 is driven by the OFF\_PSON# signal through R64 (OR/4). The source of Q5 is connected to the ATX\_V5VSB input through R1180 (OR/4). The drain of Q5 is connected to the SIO\_PSON# signal through R1180 (OR/4). The MOS\_TH\_WN# signal is connected to the drain of Q4 through R1182 (OR/4). The TH\_DIS# signal is connected to the drain of Q5 through R1183 (OR/4). The MOS\_TH\_WN# signal is also connected to the drain of Q5 through R1277 (47k).



MS-7738

Size Custom	Document Description <b>ATX PWR-Connector &amp; Front Panel</b>	Rev 10
Date: Wednesday, September 28, 2011		Sheet 29 of 47

**SVDIMM FOR DDR**

VCC5 > R298 510R/4 > SVDIMM\_5VSB > R313 10R/4 > ATX\_5VSB

(19,29) ATX\_PWR\_OK >> R292 10KST/4 > SVDIMM\_5VSB C195 0.1u/16X/4

(13,19,39) SLP\_S3# >> U21

U21: S3# S5# 5VSB\_DRV 7 5VSBDRV1 5VCC 5VSB 5VSB\_DRV 8 5VDRV1

MODE GND 5VCC\_DRV uP7501

R299 0R/4 R306 X 0R/4

(9,22,23,37,39) SLP\_S4# (19,37) SLP\_S5\_LCH#

If you use LAA and can support deep\_s3, please use SLP\_S5\_LCH#, else use SLP\_S4#.

+12V > R315 1K/6/1 > C201 22n/16X/4

C190 18n16X/4

ATX\_5VSB

S1

VCC5

Q27 SN7PNP-2003NDSG TO252-S-RH SVDIMM

G2

G3

C218 0.1u/25V/4

**UPI VOLTAGE CONSOLE**

0x24: RH=11K, RL=15K

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

5VSB 1811

R182 1K/15K/4002

C466 0.1u/16V/4

5VSB 1811

U71 UP1811BMA8

VCC BUS\_SEL OUT1 8 PCH1P5\_FB (35)

SCL SMBCLK OUT2 7 PCH1P5\_FB

SDA SMBDATA 4

GND OUT3 6

R949 15KST/4

(9,10,13,17,18,26,29,31,42) SMBCLK (9,10,13,17,18,26,29,31,42) SMBDATA

**3VA**

ATX\_5VSB

C571 1u/6.3X/4

U59 UP0111AMA5-00\_SOT23-5-HF

VIN VOUT 5 2mA

EN GND NC

C548 X 0.1u/16V/4

3VA REF

R704 10KST/4

R705 3.16KST/4

C570 4.7u/10V/B

3VA

ATX\_5VSB

R714 47K/4

C50 2N7002

(19) CP\_3VA\_OFF >>

3VSB

R747 X 0R/6

3VA

[illegible]

**SVDIMM FOR DDR**

VCC5 >> R298 510R/4 >> SVDIMM\_5VB >> R313 10R/4 >> ATX\_5VSB

(19,29) ATX\_PWR\_OK >> R292 10KST/4 >> SVDIMM\_5VB C195 0.1u/16X/4

(13,19,39) SLP\_S3# >> U21

(9,22,23,37,39) SLP\_S4# >> R299 0R/4

(19,37) SLP\_S5\_LCH# >> R306 X 0R/4

If you use LAA and can support deep\_s3,  
please use SLP\_S5\_LCH#, else use SLP\_S4#.

U21  
S3#  
S5#  
5VSB\_DRV  
MODE GND  
5VCC\_DRV  
UP7501

+12V >> R315 1K/6/1 >> C201 22n/16X/4 >> 5VDRV1

C190 18n16X/4

ATX\_5VSB

S1

VCC5

**UPI VOLTAGE CONSOLE**

0x24: RH=11K, RL=15K

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

5VSB 1811

R192 1K/15K/402

C466 0.1u/16V/4 >> 5VSB\_1811

U71  
VCC  
BUS\_SEL  
SCL  
SDA  
GND  
OUT1  
OUT2  
OUT3  
UP1811BMA8

(9,10,13,17,18,26,29,31,42) SMBCLK >> SMBCLK

(9,10,13,17,18,26,29,31,42) SMBDATA >> SMBDATA

PCH1P5\_FB (35)

**3VA**

ATX\_5VSB

C571 1u/6.3X/4

U59  
VIN  
VOUT  
EN  
GND  
NC  
UP0111AMA5-00\_SOT23-5-HF

3VA REF

C548 X 0.1u/16V/4

R704 10KST/4

R705 3.16KST/4

C570 4.7u/10Y/8

20mA

3VA

CP\_3VA\_OFF >> Q50 2N7002

3VSB

R747 X 0R/6

3VA

Used SLP\_S5# for AMT

7501 Mode  
H:Support s0/s3/s5  
L:Support s0/s3

**SVDIMM FOR DDR**

VCC5 >> R298 510R/4 >> SVDIMM\_5VB >> R313 10R/4 >> ATX\_5VSB

(19,29) ATX\_PWR\_OK >> R292 10KST/4 >> SVDIMM\_5VB C195 0.1u/16X/4

(13,19,39) SLP\_S3# >> U21

(9,22,23,37,39) SLP\_S4# >> R299 0R/4

(19,37) SLP\_S5\_LCH# >> R306 X 0R/4

If you use LAA and can support deep\_s3,  
please use SLP\_S5\_LCH#, else use SLP\_S4#.

U21  
S3#  
S5#  
5VCC  
5VSB  
5VSB\_DRV  
7  
5VSBDRV1  
MODE  
GND  
5VCC\_DRV  
8  
5VDRV1  
UP7501

R315 1K/6/1 C201 22n/16X/4 +12V

C190 18n16X/4

ATX\_5VSB

S1

VCC5

C218 0.1u/25V/4

**UPI VOLTAGE CONSOLE**

0x24: RH=11K, RL=15K

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

5VSB 1811

R192 1K/15K/4

C466 0.1u/16V/4

U71  
VCC  
BUS\_SEL  
SCL  
SDA  
GND  
OUT1  
OUT2  
OUT3  
UP1811BMA8

8 PCH1P5\_FB (35)

7 PCH1P5\_FB

3

R949 15KST/4

(9,10,13,17,18,26,29,31,42) SMBCLK >> SMBCLK

(9,10,13,17,18,26,29,31,42) SMBDATA >> SMBDATA

**3VA**

ATX\_5VSB

C571 1u/6.3X/4

U59  
UP0111AMA5-00\_SOT23-5-HF  
VIN  
VOUT  
EN  
GND  
NC

3VA REF

C548 X 0.1u/16V/4

R704 10KST/4

R705 3.16KST/4

C570 4.7u/10Y/8

20mA

3VA

CP\_3VA\_OFF >> Q50 2N7002

3VSB

R747 X 0R/6

3VA

7501 Mode  
H:Support s0/s3/s5  
L:Support s0/s3

**SVDIMM FOR DDR**

VCC5 >> R298 510R/4 >> SVDIMM\_5VB >> R313 10R/4 >> ATX\_5VSB

(19,29) ATX\_PWR\_OK >> R292 10KST/4 >> SVDIMM\_5VB C195 0.1u/16X/4

(13,19,39) SLP\_S3# >> U21

(9,22,23,37,39) SLP\_S4# >> R299 0R/4

(19,37) SLP\_S5\_LCH# >> R306 X 0R/4

If you use LAA and can support deep\_s3,  
please use SLP\_S5\_LCH#, else use SLP\_S4#.

U21  
S3#  
S5#  
5VCC  
5VSB  
5VSB\_DRV  
7  
5VSBDRV1  
MODE  
GND  
5VCC\_DRV  
8  
5VDRV1  
UP7501

R315 1K/6/1 C201 22n/16X/4 +12V

C190 18n16X/4

ATX\_5VSB

S1

VCC5

C218 0.1u/25V/4

**UPI VOLTAGE CONSOLE**

0x24: RH=11K, RL=15K

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

5VSB 1811

R192 1K/15K/402

C466 0.1u/16V/4

U71  
VCC  
BUS\_SEL  
SCL  
SDA  
GND  
OUT1  
OUT2  
OUT3  
UP1811BMA8

(9,10,13,17,18,26,29,31,42) SMBCLK >> SMBCLK

(9,10,13,17,18,26,29,31,42) SMBDATA >> SMBDATA

PCH1P5\_FB (35)

**3VA**

ATX\_5VSB

C571 1u/6.3X/4

U59  
UP0111AMA5-00\_SOT23-5-HF  
VIN  
VOUT  
EN  
GND  
NC  
C548 X 0.1u/16V/4  
3VA REF  
R704 10KST/4  
R705 3.16KST/4  
C570 4.7u/10Y/8

20mA

3VA

CP\_3VA\_OFF >> Q50 2N7002

3VSB

R747 X 0R/6

3VA

Used SLP\_S5# for AMT

7501 Mode  
H:Support s0/s3/s5  
L:Support s0/s3

[illegible]

**SVDIMM FOR DDR**

VCC5 > R298 510R/4 > SVDIMM\_5VSB > R313 10R/4 > ATX\_5VSB

(19,29) ATX\_PWR\_OK >> R292 10KST/4VDDIMM\_5V > SVDIMM\_5VSB > C195 0.1u/16X/4

(13,19,39) SLP\_S3# >> U21

(9,22,23,37,39) SLP\_S4# >> R299 0R/4

(19,37) SLP\_S5\_LCH# >> R306 X 0R/4

If you use LAA and can support deep\_s3,  
please use SLP\_S5\_LCH#, else use SLP\_S4#.

MODE GND 5VCC\_DRV uP7501

+12V > R315 1K/6/1 > C201 22n/16X/4

C190 18n16X/4

ATX\_5VSB

S1

VCC5

C218 0.1u/25V/4

**UPI VOLTAGE CONSOLE**

0x24: RH=11K, RL=15K

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

5VSB\_1811

R949 15KST/4

SMBCLK >> SMBCLK (9,10,13,17,18,26,29,31,42)

SMBDATA >> SMBDATA (9,10,13,17,18,26,29,31,42)

C466 0.1u/16V/4

5VSB\_1811

U71 UP1811BMA8

VCC BUS\_SEL OUT1 8 PCH1P5\_FB (35)

SCL OUT2 7 PCH1P5\_FB

SDA OUT3 6

GND

**3VA**

ATX\_5VSB

C571 1u/6.3X/4

U59 UP0111AMA5-00\_SOT23-5-HF

VIN VOUT

EN GND NC

X 0.1u/16V/4

3VA REF

R704 10KST/4

R705 3.16KST/4

C570 4.7u/10V/B

20mA

3VA

CP\_3VA\_OFF >> C50 2N7002

3VSB

R747 X 0R/6

3VA

Used SLP\_S# for AMT

7501 Mode  
H:Support s0/s3/s5  
L:Support s0/s3

**SVDIMM FOR DDR**

VCC5 > R298 510R/4 > SVDIMM\_5VSB > R313 10R/4 > ATX\_5VSB

(19,29) ATX\_PWR\_OK >> R292 10KST/4VDDIMM\_5V > SVDIMM\_5VSB > C195 0.1u/16X/4

(13,19,39) SLP\_S3# >> U21

(9,22,23,37,39) SLP\_S4# >> R299 0R/4

(19,37) SLP\_S5\_LCH# >> R306 X 0R/4

If you use LAA and can support deep\_s3,  
please use SLP\_S5\_LCH#, else use SLP\_S4#.

MODE GND 5VCC\_DRV uP7501

+12V > R315 1K/6/1 > C201 22n/16X/4 > 5VDRV1

C190 18n16X/4

ATX\_5VSB

S1

VCC5

C218 0.1u/25V/4

**UPI VOLTAGE CONSOLE**

0x24: RH=11K, RL=15K

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

5VSB 1811

R192 1K/15K/402

C466 0.1u/16V/4 > 5VSB 1811

U71 UP1811BMA8

VCC BUS\_SEL OUT1 8 PCH1P5\_FB (35)

SCL SMBCLK OUT2 7 PCH1P5\_FB

SDA SMBDATA 4

GND OUT3 6

R949 15KST/4

(9,10,13,17,18,26,29,31,42) SMBCLK >> SMBCLK

(9,10,13,17,18,26,29,31,42) SMBDATA >> SMBDATA

ATX\_5VSB

C571 1u/6.3X/4

U59 UP0111AMA5-00\_SOT23-5-HF

VIN VOUT 5 2mA

EN GND NC

C548 X 0.1u/16V/4

3VA REF

R704 10KST/4

R705 3.16KST/4

C570 4.7u/10Y/8

3VA

CP\_3VA\_OFF >> C50 2N7002

3VSB

R747 X 0R/6

3VA

**Used SLP\_S# for AMT**

7501 Mode  
H:Support s0/s3/s5  
L:Support s0/s3

[illegible]

**SVDIMM FOR DDR**

VCC5 ○ R298 510R/4

(19,29) ATX\_PWR\_OK >> R292 10KST/4VDDIMM\_S#

(13,19,39) SLP\_S3# >>

U21

S3# S5#

R299 0R/4

R306 X 0R/4

If you use LAA and can support deep\_s3,  
please use SLP\_S5\_LCH#,else use SLP\_S4#.

MODE GND

5VSB\_DRV

5VSDRV1

R315 1K/6/1

C201

+12V

22n/16X/4

UP7501

5VCC 5VSB

5VSBDRV1

5VSDRV1

G2

G3

S1

VCC5

C190 18n16X/4

ATX\_5VSB

O27

SNP-P2003ND5G TO252-5-RH

SVDIMM

**UPI VOLTAGE CONSOLE**

0x24: RH=11K, RL=15K

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

5VSB 1811

R182 1K/15K/402

R949 15KST/4

SMBCLK >> SMBCLK (9,10,13,17,18,26,29,31,42)

SMBDATA >> SMBDATA (9,10,13,17,18,26,29,31,42)

C466 0.1u/16V/4

5VSB 1811

U71

VCC BUS\_SEL OUT1 8

SCL OUT2 7

SDA OUT3 6

GND

UP1811BMA8

PCH1P5\_FB (35)

**3VA**

ATX\_5VSB

C571 1u6/3X/4

U59 UP0111AMA5-00\_SOT23-5-HF

VIN VOUT

EN GND NC

X 0.1u/16V/4

3VA REF

R704 10KST/4

R705 3.16KST/4

C570 4.7u/10Y/8

20mA

3VA

CP\_3VA\_OFF >> C50 2N7002

3VSB

R747 X 0R/6

3VA

**SVDIMM FOR DDR**

VCC5 >> R298 510R/4 >> SVDIMM\_5VB >> R313 10R/4 >> ATX\_5VSB

(19,29) ATX\_PWR\_OK >> R292 10KST/4 >> SVDIMM\_5VB C195 0.1u/16X/4

(13,19,39) SLP\_S3# >> U21

(9,22,23,37,39) SLP\_S4# >> R299 0R/4

(19,37) SLP\_S5\_LCH# >> R306 X 0R/4

If you use LAA and can support deep\_s3,  
please use SLP\_S5\_LCH#, else use SLP\_S4#.

U21  
S3#  
S5#  
5VCC  
5VSB  
5VSB\_DRV  
7  
5VSBDRV1  
MODE  
GND  
5VCC\_DRV  
8  
5VDRV1  
UP7501

R315 1K/6/1 C201 22n/16X/4 +12V

C190 18n16X/4

ATX\_5VSB

S1

VCC5

C218 0.1u/25V/4

**UPI VOLTAGE CONSOLE**

0x24: RH=11K, RL=15K

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

5VSB 1811

R192 1K/15K/402

C466 0.1u/16V/4

U71  
VCC  
BUS\_SEL  
SCL  
SDA  
GND  
OUT1  
OUT2  
OUT3  
UP1811BMA8

(9,10,13,17,18,26,29,31,42) SMBCLK >> SMBCLK

(9,10,13,17,18,26,29,31,42) SMBDATA >> SMBDATA

PCH1P5\_FB (35)

**3VA**

ATX\_5VSB

C571 1u/6.3X/4

U59  
UP0111AMA5-00\_SOT23-5-HF  
VIN  
VOUT  
EN  
NC  
C548 X 0.1u/16V/4  
3VA REF  
R704 10KST/4  
R705 3.16KST/4  
C570 4.7u/10Y/8  
20mA  
3VA

CP\_3VA\_OFF >> Q50 2N7002

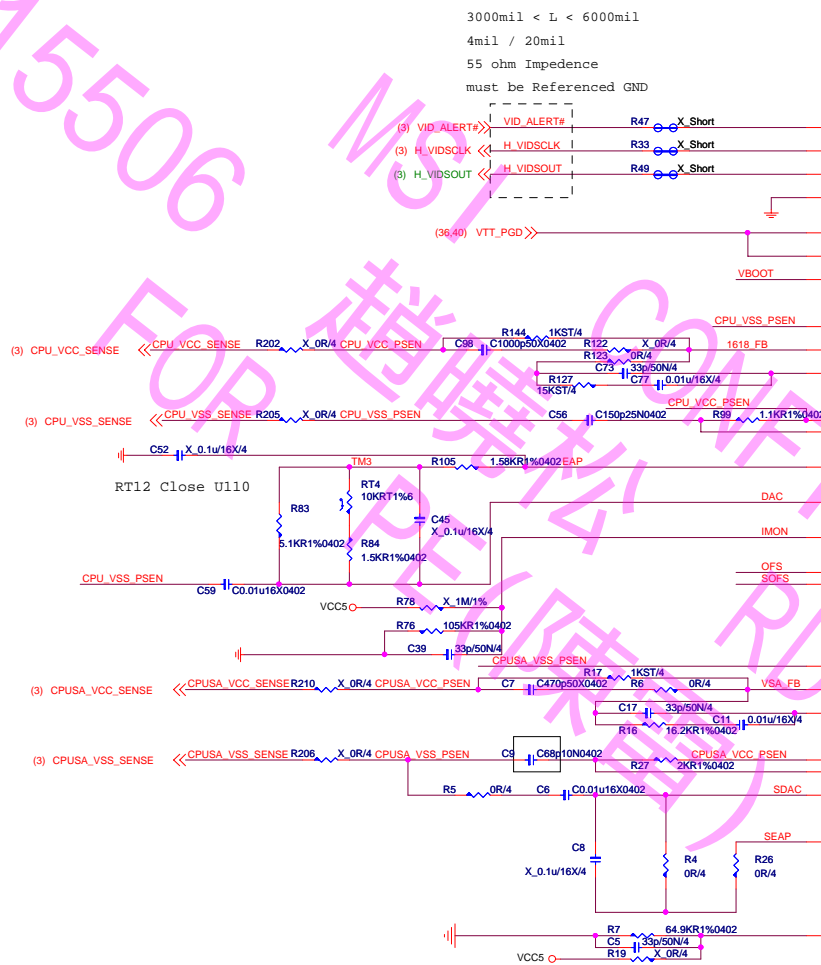
R747 X 0R/6

3VSB

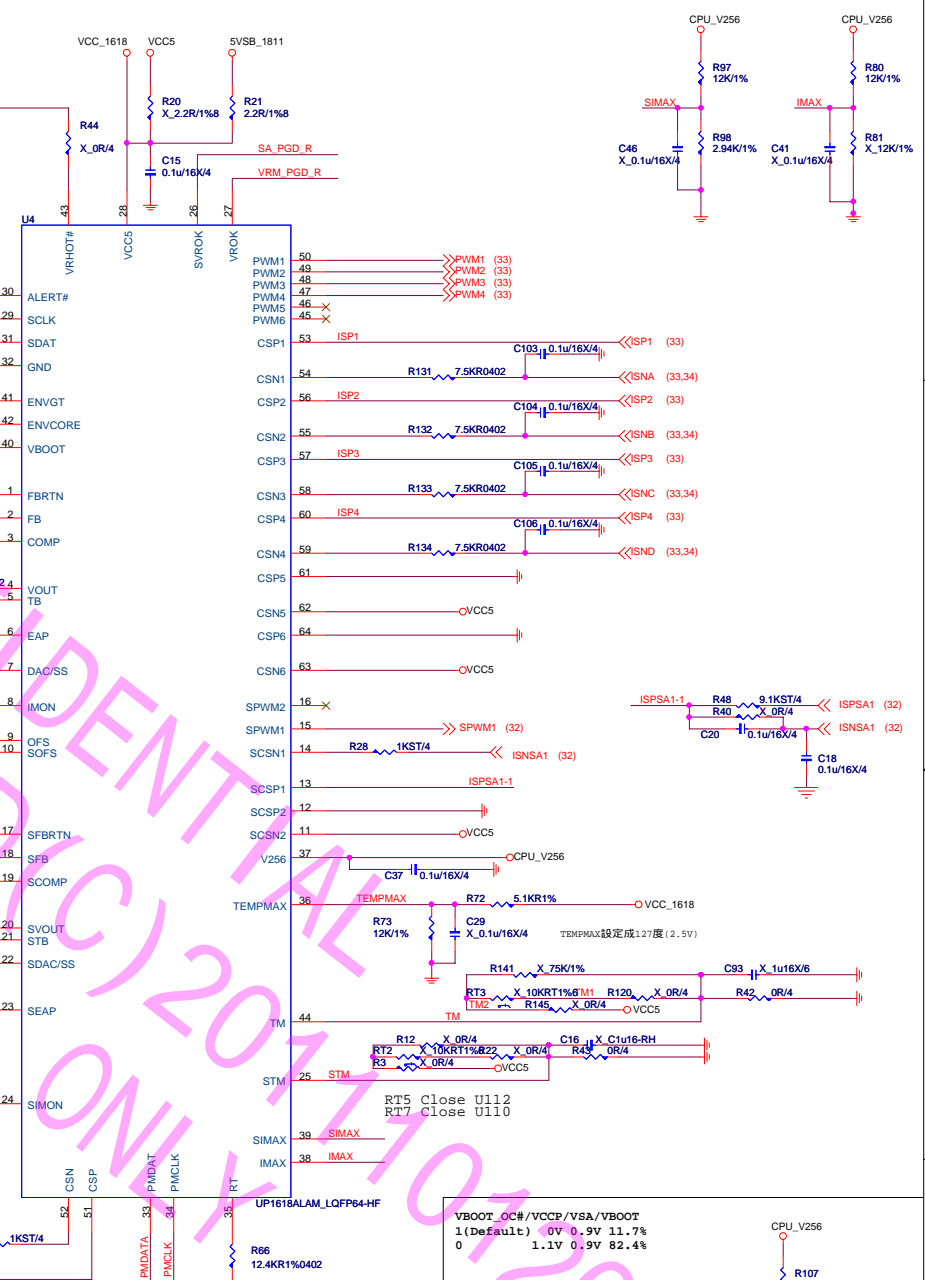
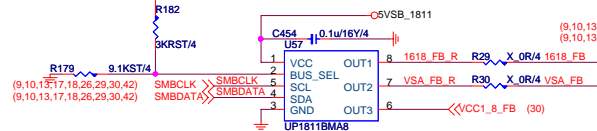
3VA

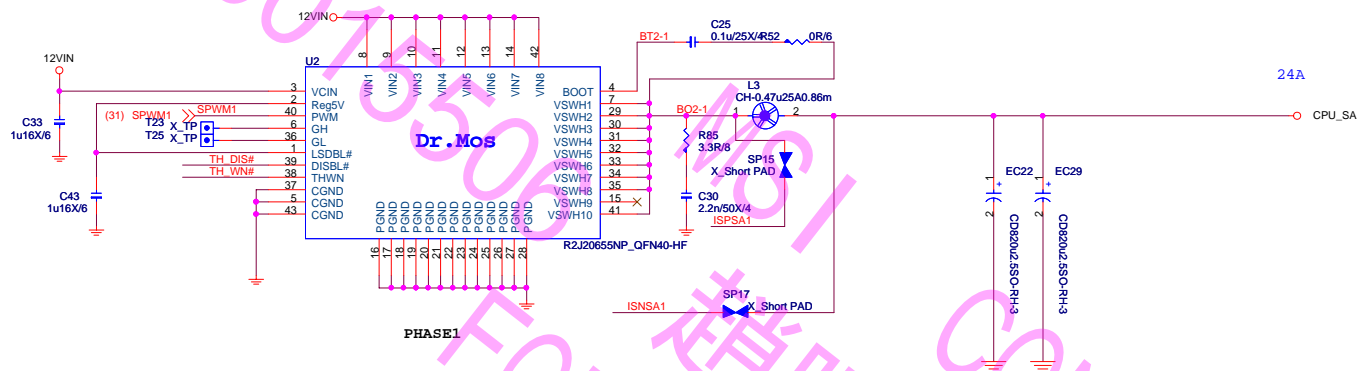
The schematic diagram illustrates the power and signal connections for the NN-CMKT3904 microcontroller. The microcontroller is represented by a block with pins 1 through 6. The connections are as follows:

- Power Connections:**
  - 3VSB:** Connected to pin 1 through resistor R104 (10KST/4).
  - VCC3:** Connected to pin 6 through resistor R82 (4.7K/4).
  - SA\_PGD (30):** Connected to pin 5 through resistor R116 (4.7K/4).
  - CPU\_VTT:** Connected to pin 2 through resistor R112 (1KR/4).
  - CPUSA\_VSS\_PSEN:** Connected to pin 3 through resistor R1230 (0R/4) and capacitor C1097 (X\_0.1u/16X/4).
  - CPUSA\_VCC\_PSEN:** Connected to pin 4 through resistor R1231 (0R/4) and capacitor C1098 (X\_0.1u/16X/4).
  - CPU\_VSS\_PSEN:** Connected to pin 1 through resistor R162 (0R/4) and capacitor C97 (X\_0.1u/16X/4).
  - CPU\_VCC\_PSEN:** Connected to pin 2 through resistor R161 (0R/4) and capacitor C99 (X\_0.1u/16X/4).
  - VCCP:** Connected to pin 3 through resistor R161 (0R/4) and capacitor C108 (X\_0.1u/16X/4).
  - VCC\_1618:** Connected to pin 4 through resistor R1086 (X\_9.1KST/4).
  - SOFS:** Connected to pin 5 through resistor R1116 (X\_9.1KST/4).
- Signal Connections:**
  - CPU\_SA:** Connected to pin 6 through resistor R1231 (0R/4).
  - SA\_PGD:** Connected to pin 5 through resistor R116 (4.7K/4).
- Other Components:**
  - R54 (110R):** Connected to CPU\_VTT and H\_VIDSOUT.
  - R32 (56/1%):** Connected to CPU\_VTT and H\_VIDSCLK.
  - C65 (X\_0.1u/16X/4):** Connected to CPU\_VTT and ground.



0x22:RH=3K,RL=9.1K						
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%





(13,29,34,40) TH\_WN# << TH\_WN#

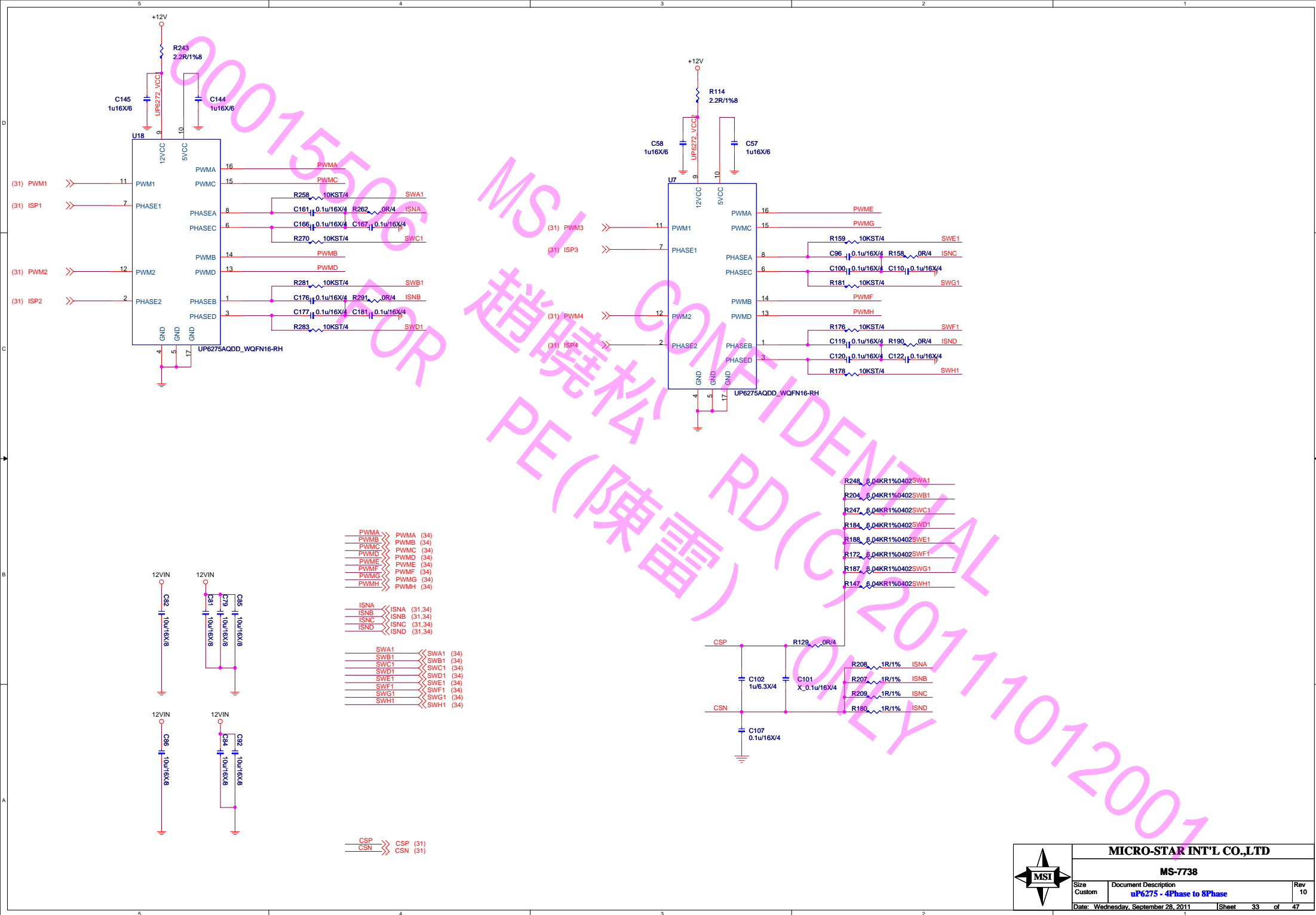
(29,34,40) TH\_DIS# << TH\_DIS#

12VIN C1 10u/16X/8

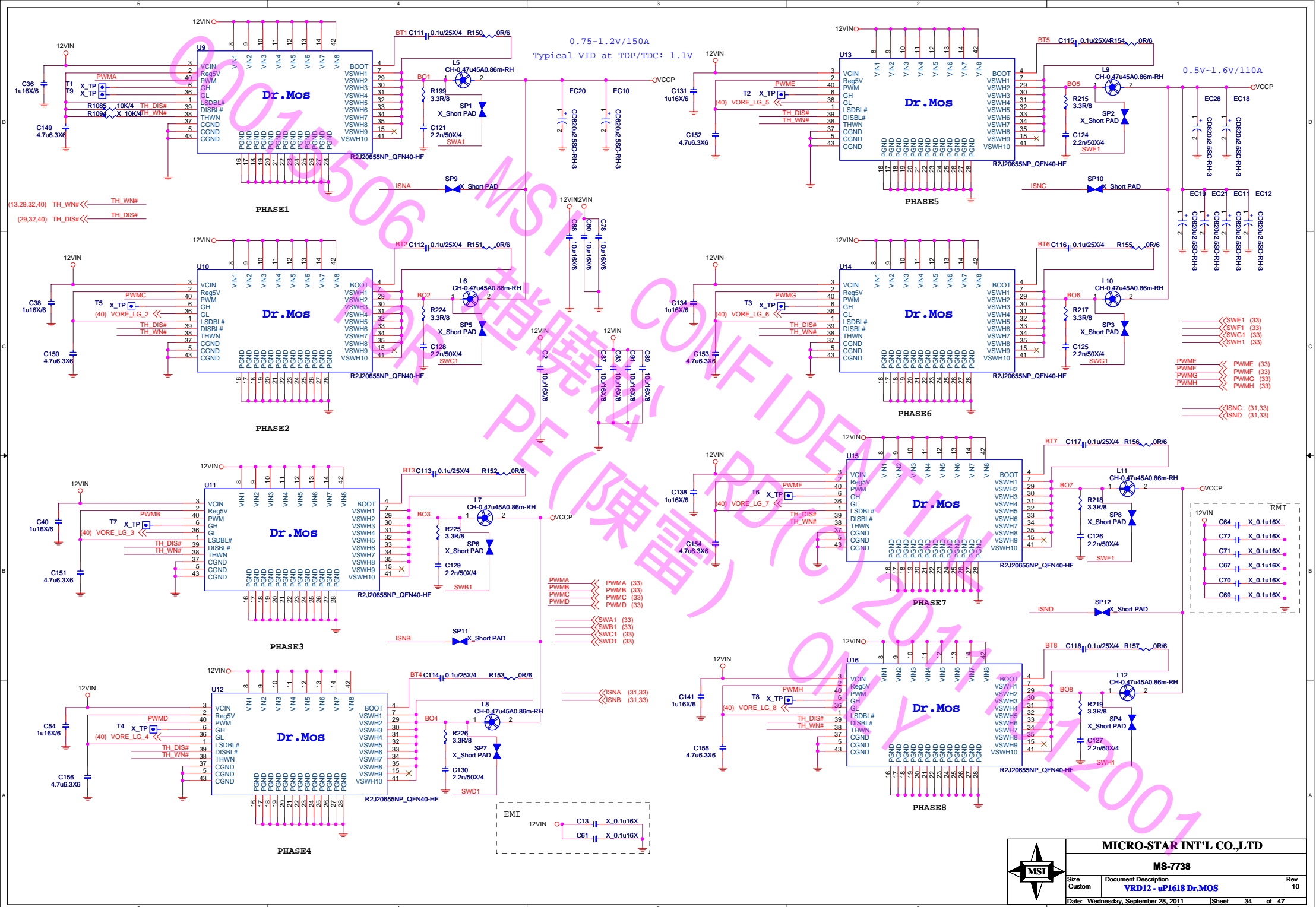
12VIN C3 10u/16X/8

(31) ISPSA1 >>

(31) ISNSA1 >>





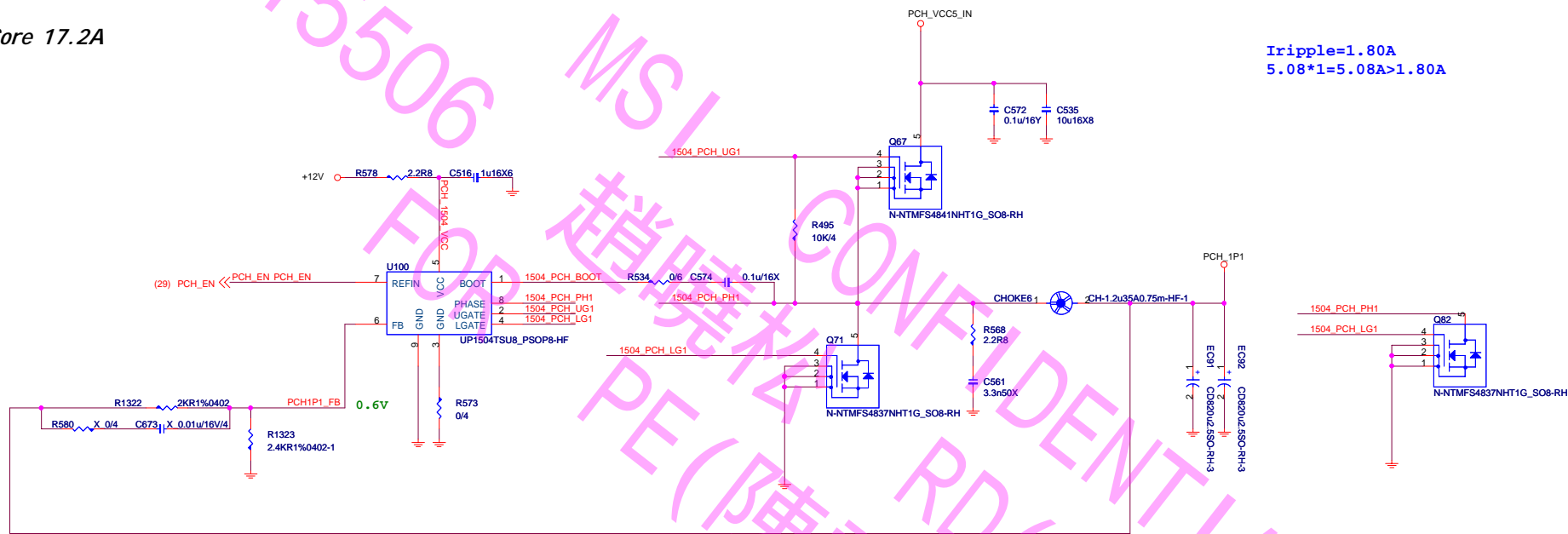


PCH Core 17.2A

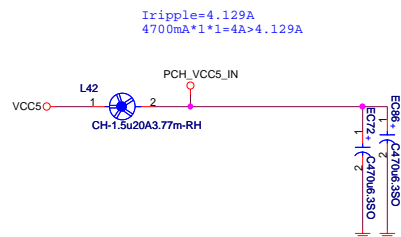
Tripple=1.80A  
5.08\*1=5.08A>1.80A

PCH Core 17.2A

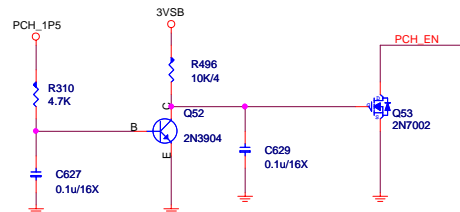
Tripple=1.80A  
5.08\*1=5.08A>1.80A



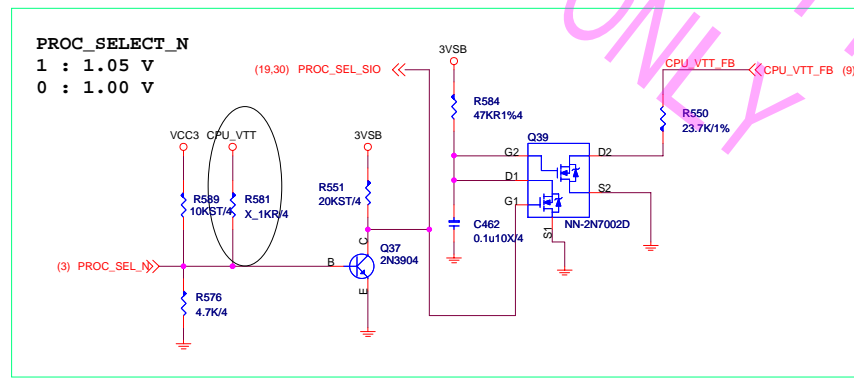
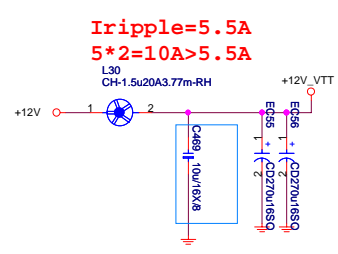
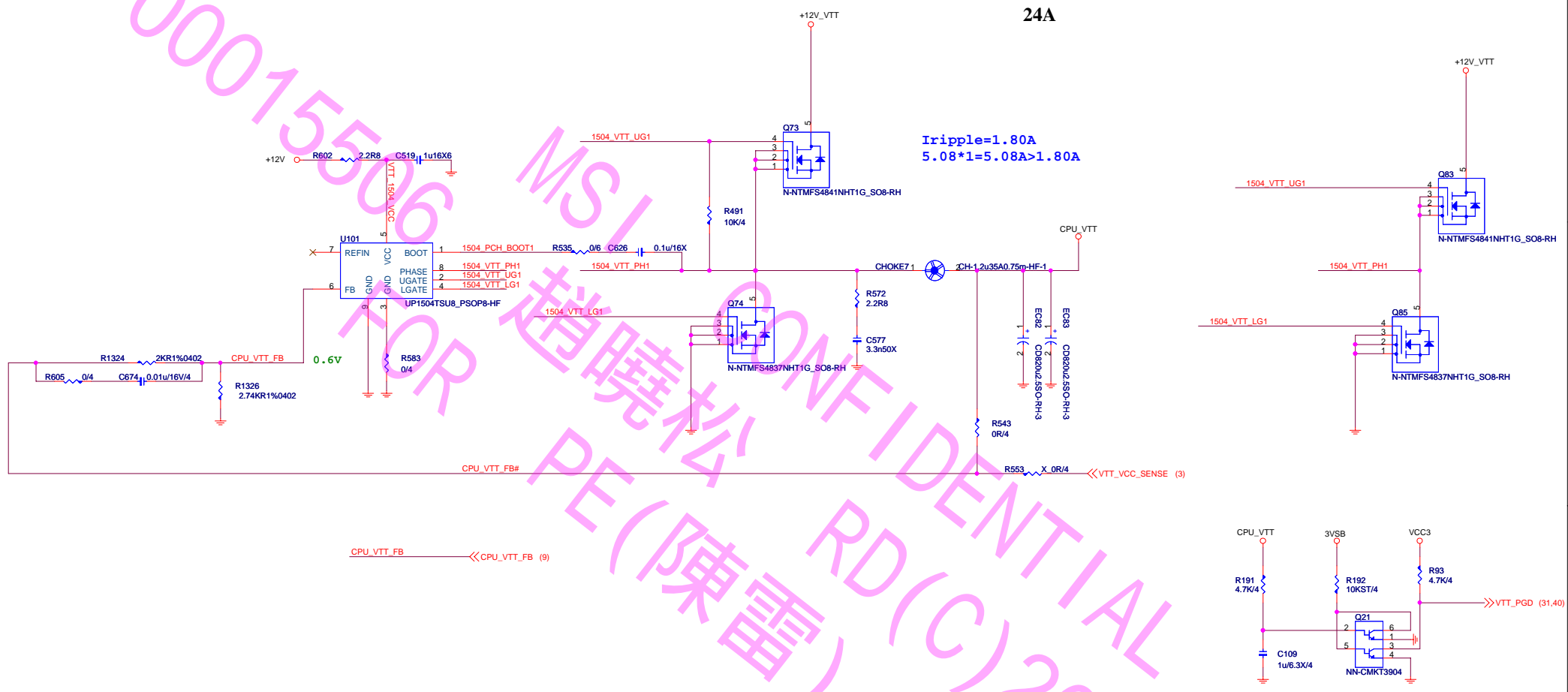
PCH1P1\_FB << PCH1P1\_FB (30)



Tripple=4.129A  
4700mA\*1\*1=4A>4.129A



CPU\_VTT:1.05  
CPU\_VTT 22A  
(8.5A FOR CPU)



*DDR3\_1.5V* 20A

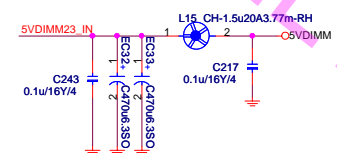
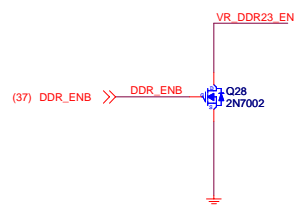
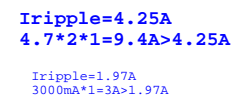


MICRO-STAR INT'L CO.,LTD

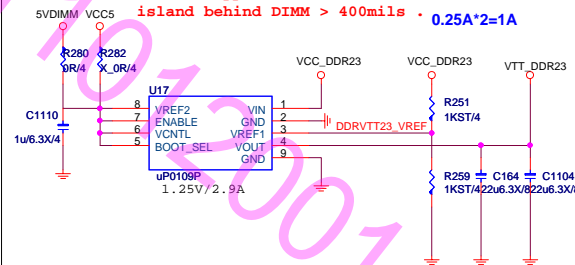
MS-7738

Size Custom	Document Description <b>DDR01-uP6212 2-Phase</b>	Rev 10
Date: Wednesday, September 28, 2011		Sheet 37 of 47

**DDR3\_1.5V 20A**



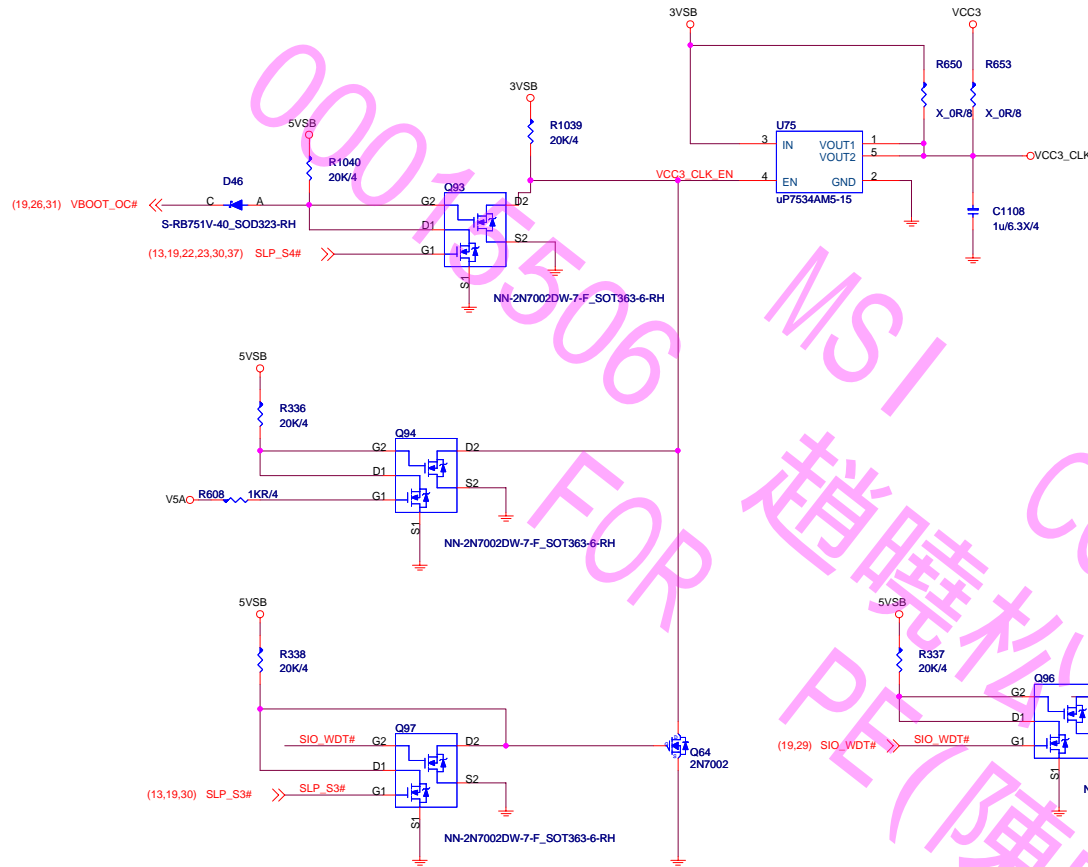
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .  $0.25A \times 2 = 1A$



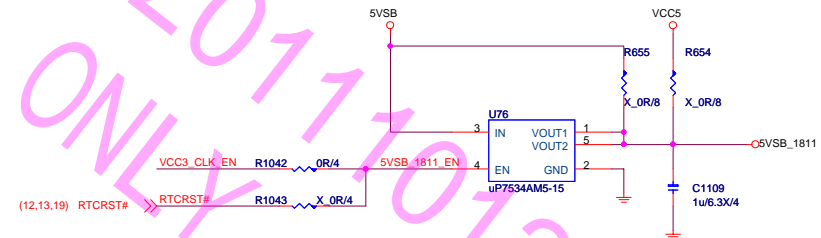
MS-7738

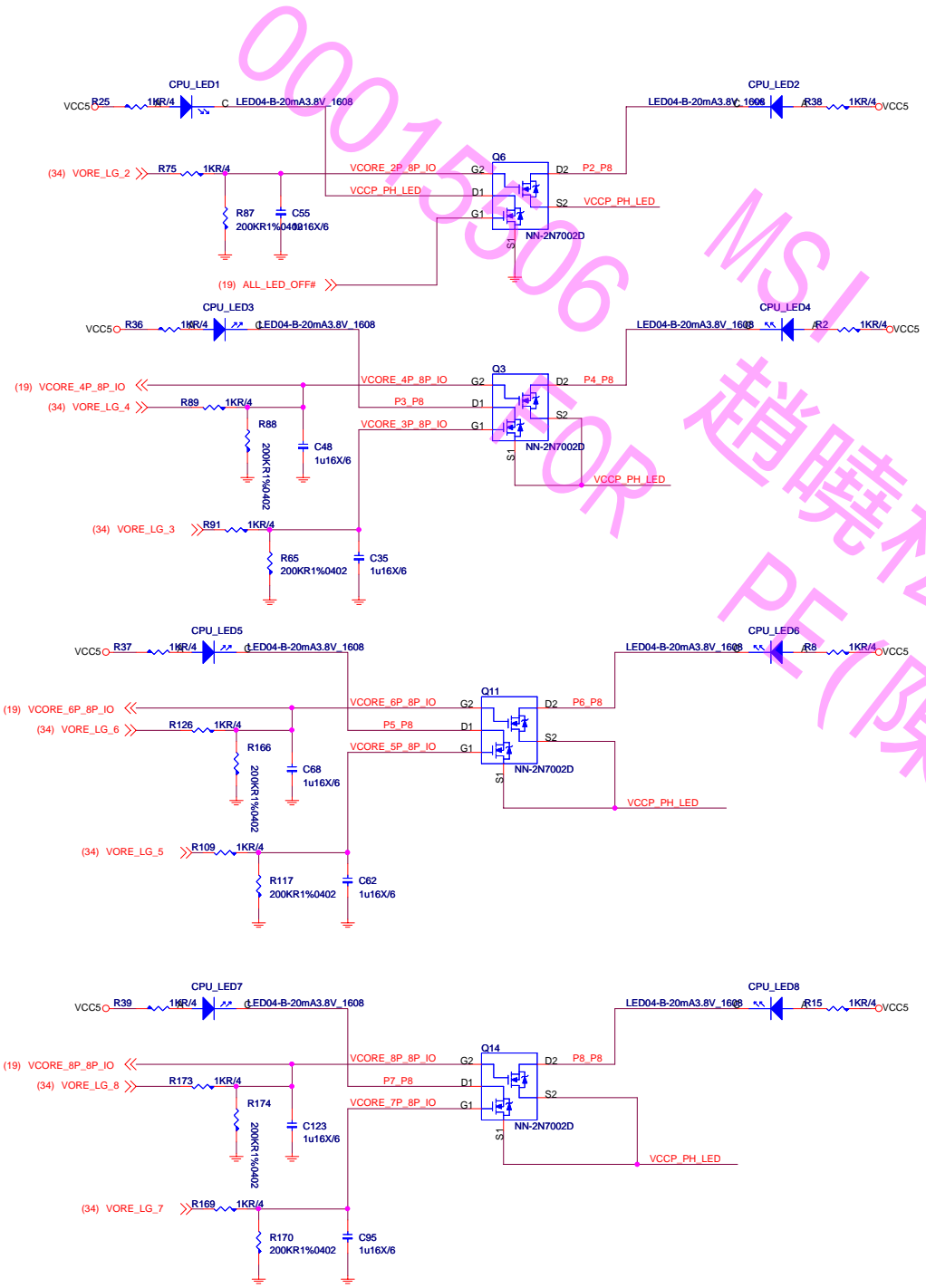
Size Custom	Document Description <b>DDR23-uP6212 2-Phase</b>	Rev 10
Date: Wednesday, September 28, 2011		Sheet 38 of 47



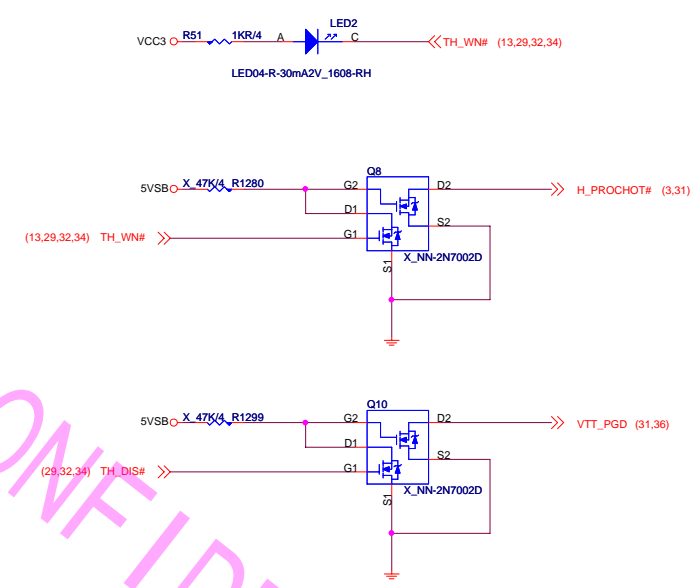


MSI CONFIDENTIAL  
FOR 趙曉松 RD(C) 20111012001  
PE (陳雷)






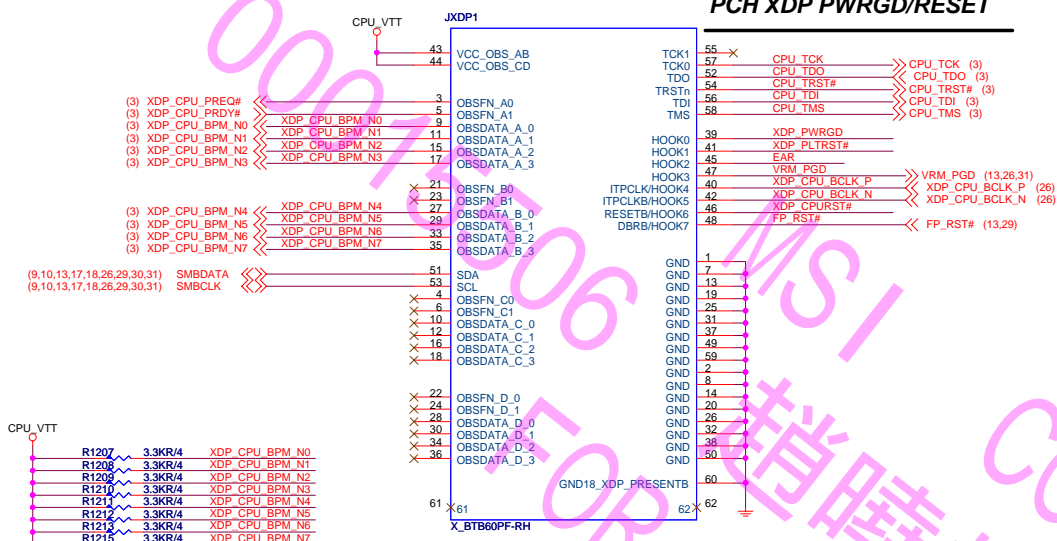
Warning LED



00015506 MSI CONFIDENTIAL  
FOR 趙曉松 RD(C)20111012001  
PE(陳雷) ONLY

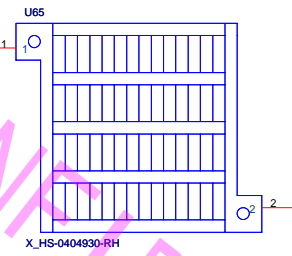
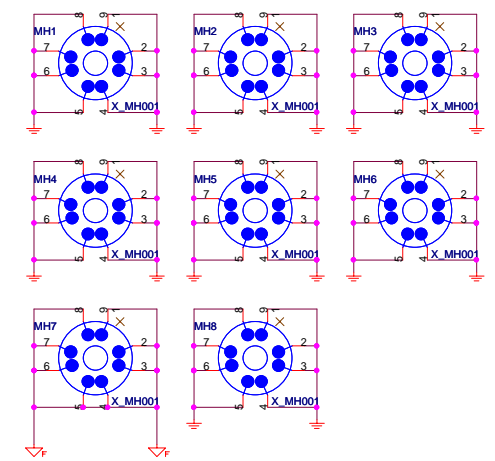
	MICRO-STAR INT'L CO.,LTD		
	MS-7738		
	Size Custom	Document Description <b>PHASE Dropping &amp; LED</b>	Rev 10
	Date: Friday, August 26, 2011		Sheet 41 of 47

PCH XDP PWRGD/RESET

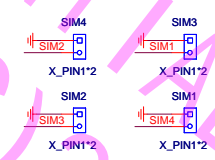


OPT	BOM	Function
A	601-7738-01S	
B	601-7738-XXX	

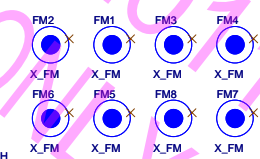
Mounting Holes



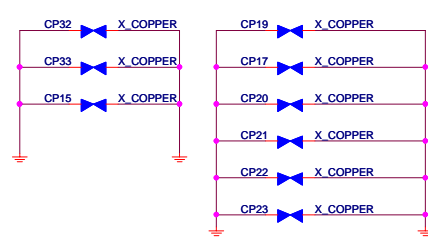
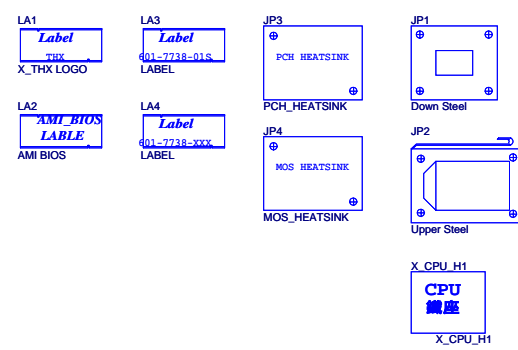
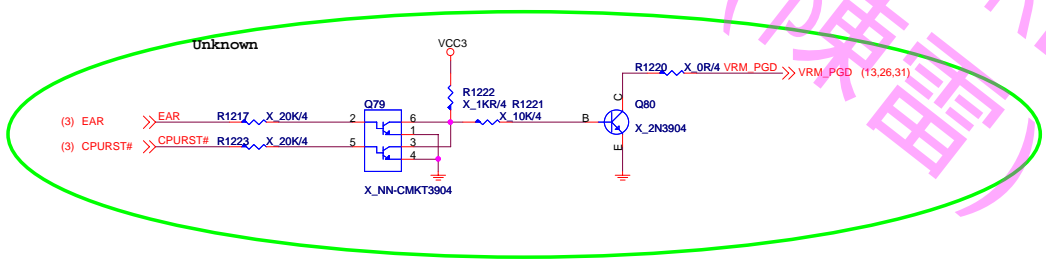
Simulation



Optical Fiducial Marks-120



Optical Fiducial Marks-100



PD0-0773811-E48, 競華, 23, 寶安恩斯通廠 (MSIS), 8, Coffee\_black  
 PD0-0773811-E48, 競華, 377, 寶安恩斯通廠 (MSIS), 8, Coffee\_black  
 PD0-0773811-T53, 健鼎無錫, 23, 寶安恩斯通廠 (MSIS), 8, Coffee\_black  
 PD0-0773811-T53, 健鼎無錫, 377, 寶安恩斯通廠 (MSIS), 8, Coffee\_black

**MICRO-STAR INT'L CO.,LTD**

**MS-7738**

Size Custom Document Description **XDP / Manual Parts** Rev 10

Date: Wednesday, September 28, 2011 Sheet 42 of 47